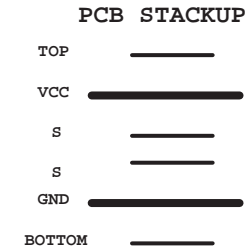


Project code: 91.4AJ01.001
PCB P/N : 48.4AJ01.001
REVISION : 08208-1



<Core Design>

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BLOCK DIAGRAM			
Size	Document Number	Rev	
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Date:	Monday, October 27, 2008	Sheet 1 of 55	

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C									
B									
A									

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

HISTORY

Size

A3

Document Number

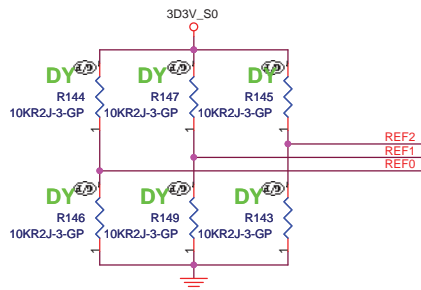
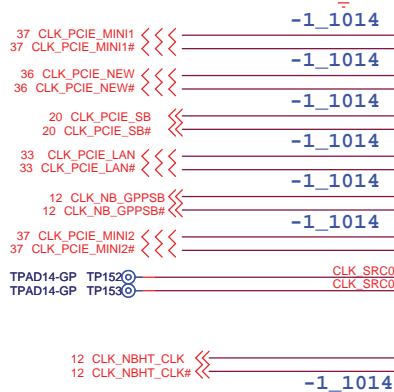
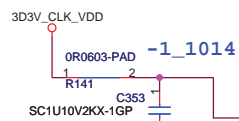
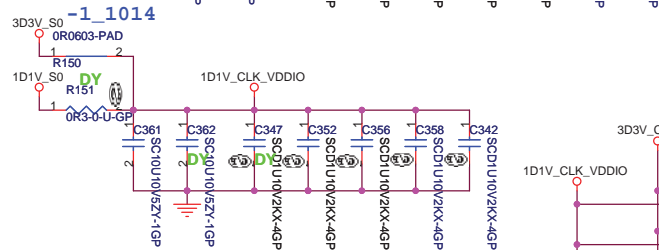
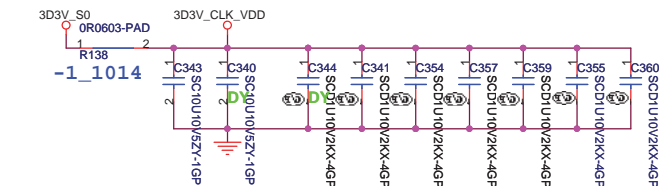
Big Bear 2A

Rev

SA

Date: Monday, October 27, 2008

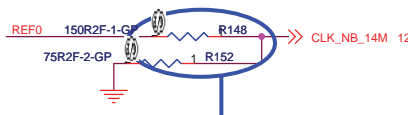
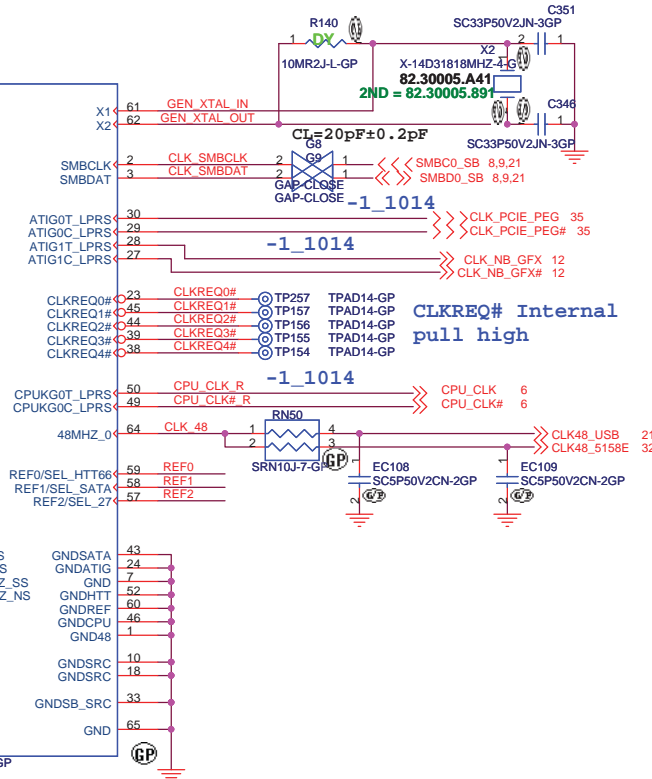
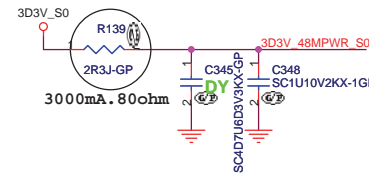
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SEL_27	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
REF2	0*	100MHz differential spreading SRC clock
SEL_SATA	1	100MHz non-spreading differential SATA clock
REF1	0*	100MHz differential spreading SRC clock
SEL_HTT66	1	66MHz 3.3V single ended HTT clock
REF0	0*	100MHz differential HTT clock

* default

CPU_CLK (200MHz)



OSC 14M NB
RS780M 1.1V 158R/90.9F

Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIe reference clocks. By default, chip will configured as input mode, BIOS can program it to output mode.

<Core Design>

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CLKGEN_ICS9LPRS480

Size

A3

Document Number

Big Bear 2A

Date

Monday, October 27, 2008

Rev

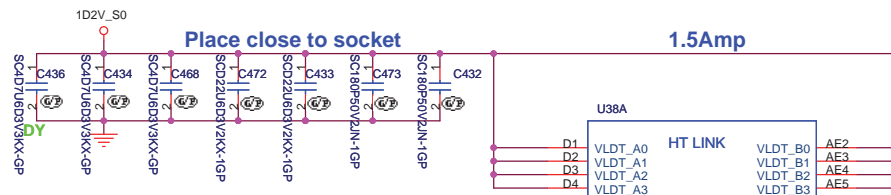
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55



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V

11 HT_NB_CPU_CAD_H0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	11 HT_CPU_NB_CAD_H0
11 HT_NB_CPU_CAD_L0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	11 HT_CPU_NB_CAD_L0
11 HT_NB_CPU_CAD_H1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	11 HT_CPU_NB_CAD_H1
11 HT_NB_CPU_CAD_L1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	11 HT_CPU_NB_CAD_L1
11 HT_NB_CPU_CAD_H2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	11 HT_CPU_NB_CAD_H2
11 HT_NB_CPU_CAD_L2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	11 HT_CPU_NB_CAD_L2
11 HT_NB_CPU_CAD_H3	H1	L0_CADIN_H3	L0_CADOUT_H3	AA2	11 HT_CPU_NB_CAD_H3
11 HT_NB_CPU_CAD_L3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	11 HT_CPU_NB_CAD_L3
11 HT_NB_CPU_CAD_H4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	11 HT_CPU_NB_CAD_H4
11 HT_NB_CPU_CAD_L4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	11 HT_CPU_NB_CAD_L4
11 HT_NB_CPU_CAD_H5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	11 HT_CPU_NB_CAD_H5
11 HT_NB_CPU_CAD_L5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	11 HT_CPU_NB_CAD_L5
11 HT_NB_CPU_CAD_H6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	11 HT_CPU_NB_CAD_H6
11 HT_NB_CPU_CAD_L6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	11 HT_CPU_NB_CAD_L6
11 HT_NB_CPU_CAD_H7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	11 HT_CPU_NB_CAD_H7
11 HT_NB_CPU_CAD_L7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	11 HT_CPU_NB_CAD_L7
11 HT_NB_CPU_CAD_H8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD4	11 HT_CPU_NB_CAD_H8
11 HT_NB_CPU_CAD_L8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	11 HT_CPU_NB_CAD_L8
11 HT_NB_CPU_CAD_H9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	11 HT_CPU_NB_CAD_H9
11 HT_NB_CPU_CAD_L9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	11 HT_CPU_NB_CAD_L9
11 HT_NB_CPU_CAD_H10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	11 HT_CPU_NB_CAD_H10
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11 HT_NB_CPU_CAD_H12	K3	L0_CADIN_H12	L0_CADOUT_H12	V5	11 HT_CPU_NB_CAD_H12
11 HT_NB_CPU_CAD_L12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	11 HT_CPU_NB_CAD_L12
11 HT_NB_CPU_CAD_H13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	11 HT_CPU_NB_CAD_H13
11 HT_NB_CPU_CAD_L13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	11 HT_CPU_NB_CAD_L13
11 HT_NB_CPU_CAD_H14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	11 HT_CPU_NB_CAD_H14
11 HT_NB_CPU_CAD_L14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	11 HT_CPU_NB_CAD_L14
11 HT_NB_CPU_CAD_H15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	11 HT_CPU_NB_CAD_H15
11 HT_NB_CPU_CAD_L15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	11 HT_CPU_NB_CAD_L15
11 HT_NB_CPU_CLK_H0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	11 HT_CPU_NB_CLK_H0
11 HT_NB_CPU_CLK_L0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	11 HT_CPU_NB_CLK_L0
11 HT_NB_CPU_CLK_H1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	11 HT_CPU_NB_CLK_H1
11 HT_NB_CPU_CLK_L1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	11 HT_CPU_NB_CLK_L1
11 HT_NB_CPU_CTL_H0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	11 HT_CPU_NB_CTL_H0
11 HT_NB_CPU_CTL_L0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	11 HT_CPU_NB_CTL_L0
11 HT_NB_CPU_CTL_H1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	11 HT_CPU_NB_CTL_H1
11 HT_NB_CPU_CTL_L1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	11 HT_CPU_NB_CTL_L1

SKT-CPU638P-GP-U2
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2ND = 62.10055.251
SKT-BGA638H176

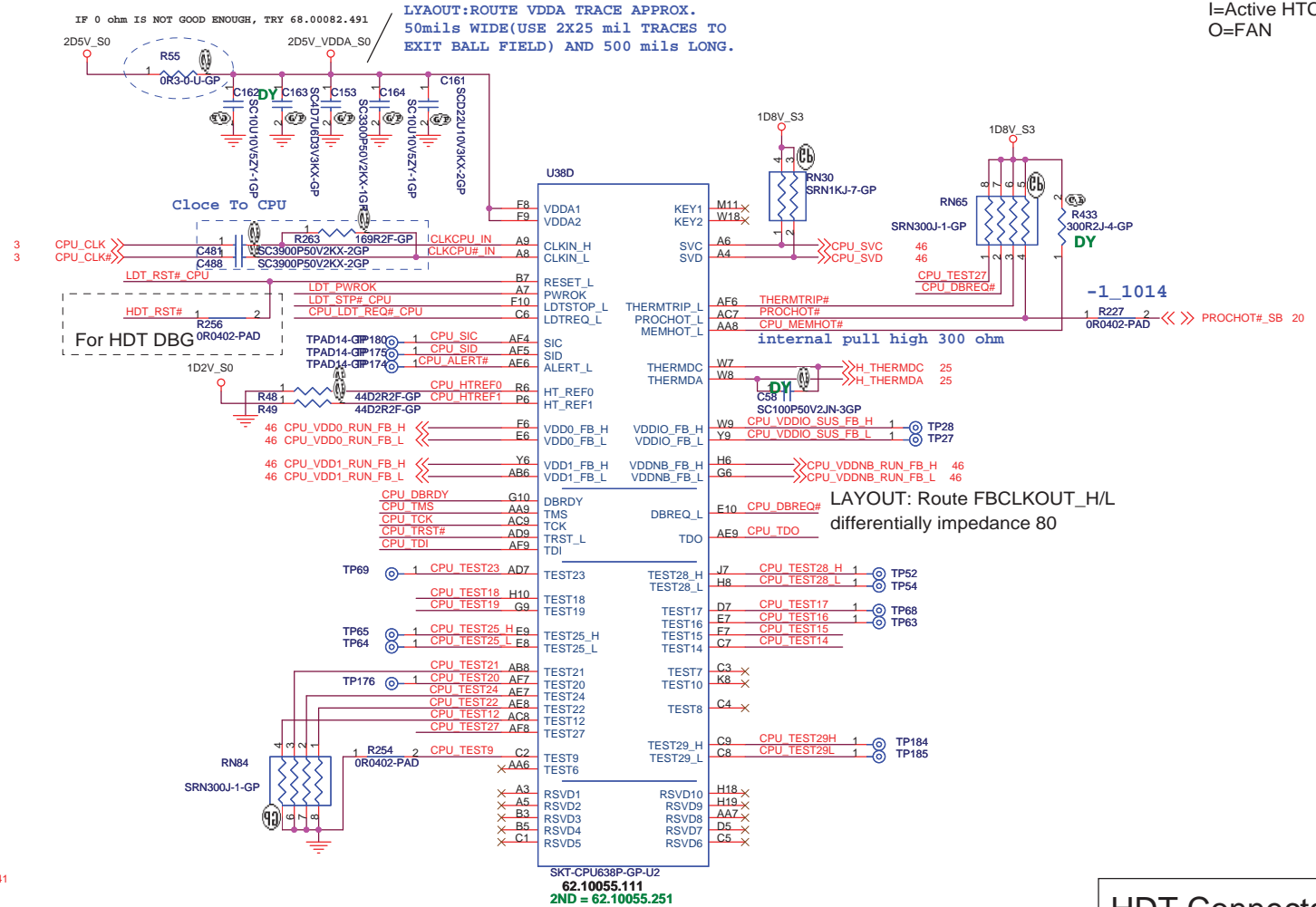
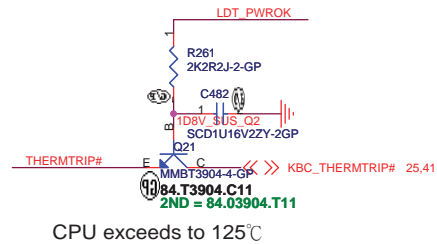
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Title CPU_HT_LINK I/F (1/4)

Size A3 Document Number Big Bear 2A Rev SA

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The Processor has reached a preset maximum operating temperature. 100°C
I=Active HTC
O=FAN

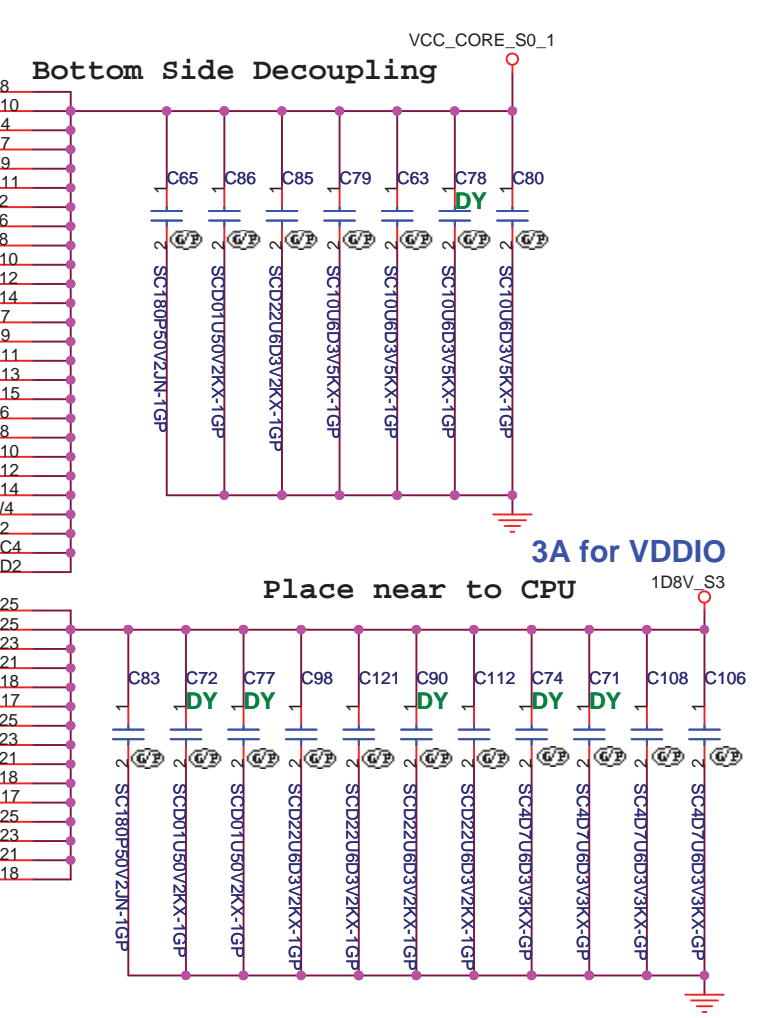
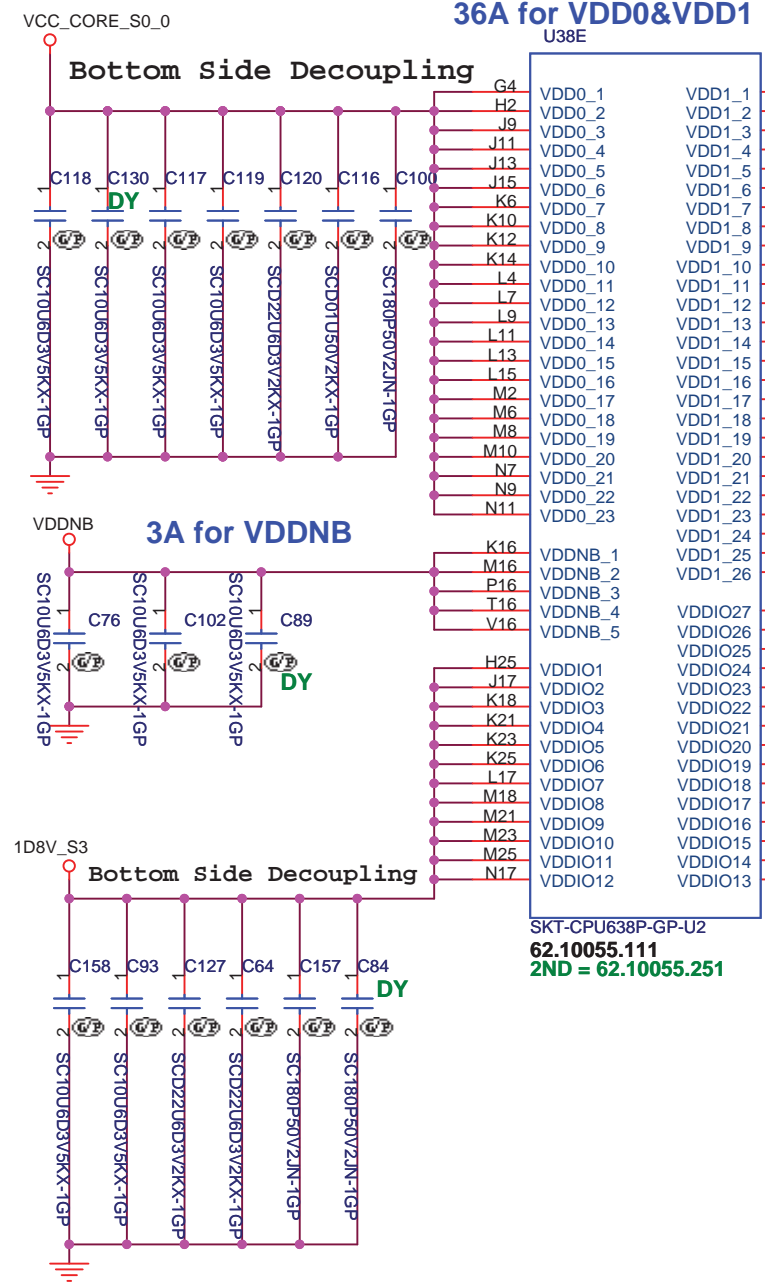
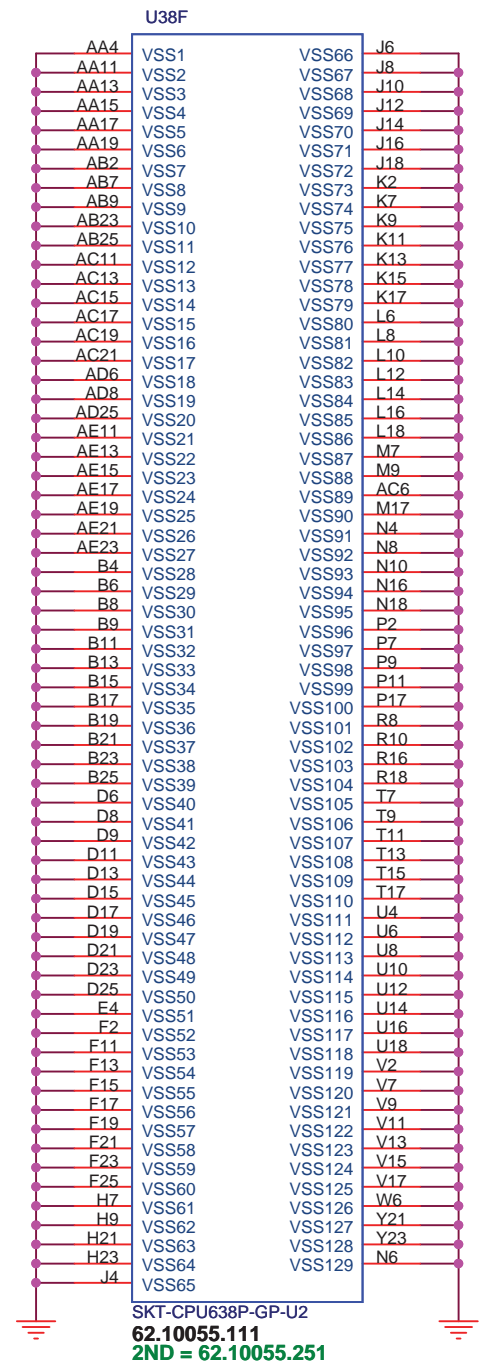
HDT Connectors

CPU DBREQ#	1	TP17	TPAD14-GP
CPU DBRDY	1	TP50	TPAD14-GP
CPU TCK	1	TP21	TPAD14-GP
CPU TMS	1	TP23	TPAD14-GP
CPU TDI	1	TP20	TPAD14-GP
CPU TRST#	1	TP19	TPAD14-GP
CPU TDO	1	TP18	TPAD14-GP
1D8V_S3	1	TP29	TPAD14-GP
HDT_RST#	1	TP183	TPAD14-GP

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Title			
CPU_Control&Debug_(3/4)			
Size	Document Number	Rev	
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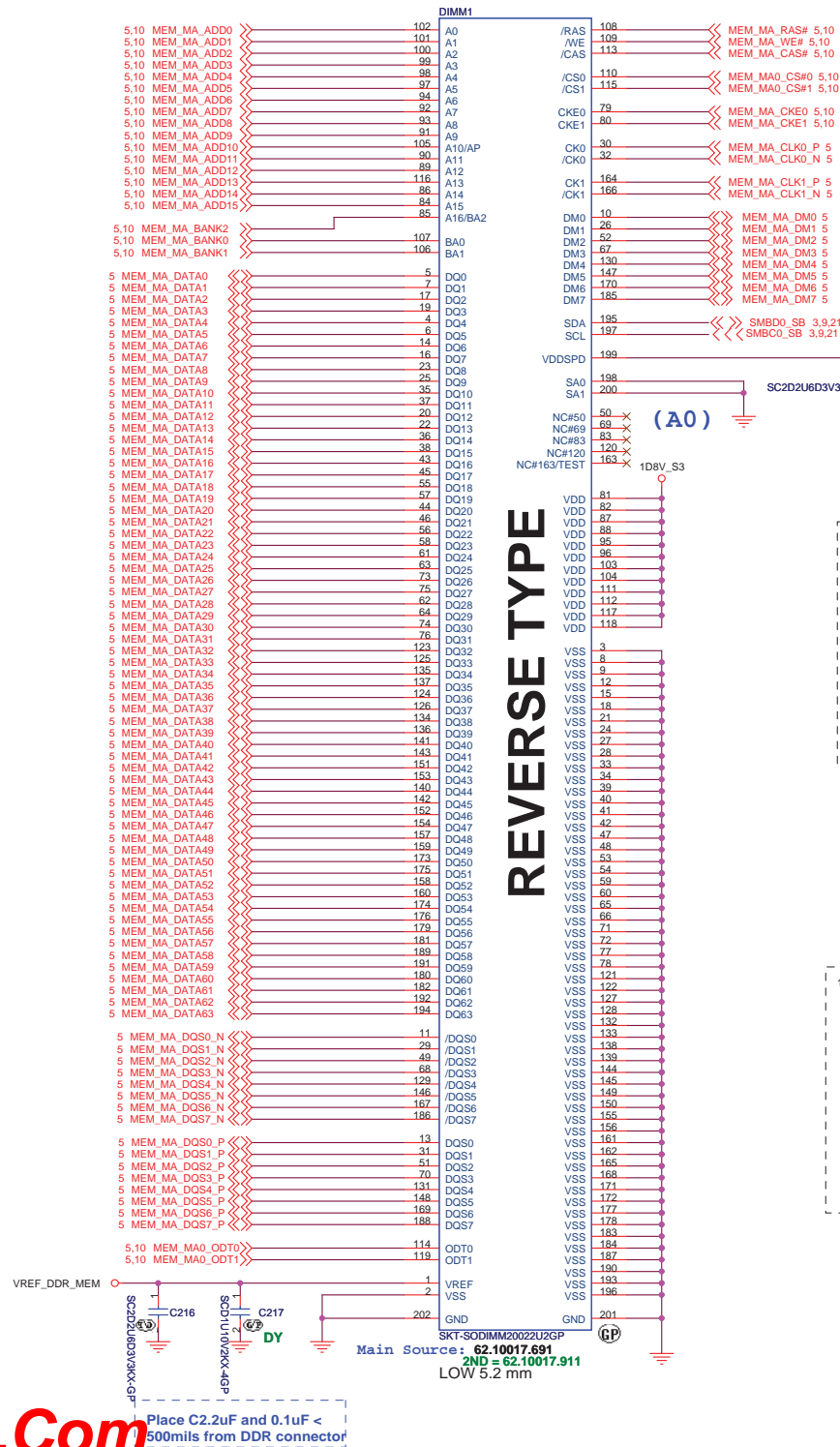


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Title: **CPU_Power_(4/4)**

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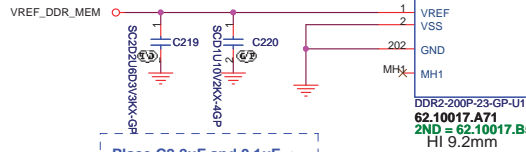
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5,10 MEM_MB_ADD2 >> 100 A2
5,10 MEM_MB_ADD3 >> 98 A3
5,10 MEM_MB_ADD4 >> 97 A4
5,10 MEM_MB_ADD5 >> 94 A5
5,10 MEM_MB_ADD6 >> 92 A6
5,10 MEM_MB_ADD7 >> 93 A7
5,10 MEM_MB_ADD8 >> 91 A8
5,10 MEM_MB_ADD9 >> 105 A9
5,10 MEM_MB_ADD10 >> 90 A10/AP
5,10 MEM_MB_ADD11 >> 89 A11
5,10 MEM_MB_ADD12 >> 116 A12
5,10 MEM_MB_ADD13 >> 86 A13
5,10 MEM_MB_ADD14 >> 84 A14
5,10 MEM_MB_ADD15 >> 85 A15
5,10 MEM_MB_BANK2 >> 107 BA0
5,10 MEM_MB_BANK0 >> 106 BA1
5,10 MEM_MB_BANK1 >> 106 BA1

5 MEM_MB_DATA0 >> 5 DQ0
5 MEM_MB_DATA1 >> 7 DQ1
5 MEM_MB_DATA2 >> 17 DQ2
5 MEM_MB_DATA3 >> 19 DQ3
5 MEM_MB_DATA4 >> 4 DQ4
5 MEM_MB_DATA5 >> 6 DQ5
5 MEM_MB_DATA6 >> 14 DQ6
5 MEM_MB_DATA7 >> 16 DQ7
5 MEM_MB_DATA8 >> 23 DQ8
5 MEM_MB_DATA9 >> 25 DQ9
5 MEM_MB_DATA10 >> 35 DQ10
5 MEM_MB_DATA11 >> 37 DQ11
5 MEM_MB_DATA12 >> 20 DQ12
5 MEM_MB_DATA13 >> 22 DQ13
5 MEM_MB_DATA14 >> 36 DQ14
5 MEM_MB_DATA15 >> 38 DQ15
5 MEM_MB_DATA16 >> 43 DQ16
5 MEM_MB_DATA17 >> 45 DQ17
5 MEM_MB_DATA18 >> 55 DQ18
5 MEM_MB_DATA19 >> 57 DQ19
5 MEM_MB_DATA20 >> 44 DQ20
5 MEM_MB_DATA21 >> 46 DQ21
5 MEM_MB_DATA22 >> 56 DQ22
5 MEM_MB_DATA23 >> 58 DQ23
5 MEM_MB_DATA24 >> 61 DQ24
5 MEM_MB_DATA25 >> 62 DQ25
5 MEM_MB_DATA26 >> 73 DQ26
5 MEM_MB_DATA27 >> 75 DQ27
5 MEM_MB_DATA28 >> 62 DQ28
5 MEM_MB_DATA29 >> 64 DQ29
5 MEM_MB_DATA30 >> 74 DQ30
5 MEM_MB_DATA31 >> 76 DQ31
5 MEM_MB_DATA32 >> 123 DQ32
5 MEM_MB_DATA33 >> 125 DQ33
5 MEM_MB_DATA34 >> 135 DQ34
5 MEM_MB_DATA35 >> 137 DQ35
5 MEM_MB_DATA36 >> 124 DQ36
5 MEM_MB_DATA37 >> 126 DQ37
5 MEM_MB_DATA38 >> 134 DQ38
5 MEM_MB_DATA39 >> 136 DQ39
5 MEM_MB_DATA40 >> 141 DQ40
5 MEM_MB_DATA41 >> 143 DQ41
5 MEM_MB_DATA42 >> 151 DQ42
5 MEM_MB_DATA43 >> 153 DQ43
5 MEM_MB_DATA44 >> 140 DQ44
5 MEM_MB_DATA45 >> 142 DQ45
5 MEM_MB_DATA46 >> 152 DQ46
5 MEM_MB_DATA47 >> 154 DQ47
5 MEM_MB_DATA48 >> 157 DQ48
5 MEM_MB_DATA49 >> 159 DQ49
5 MEM_MB_DATA50 >> 173 DQ50
5 MEM_MB_DATA51 >> 175 DQ51
5 MEM_MB_DATA52 >> 158 DQ52
5 MEM_MB_DATA53 >> 160 DQ53
5 MEM_MB_DATA54 >> 174 DQ54
5 MEM_MB_DATA55 >> 176 DQ55
5 MEM_MB_DATA56 >> 179 DQ56
5 MEM_MB_DATA57 >> 181 DQ57
5 MEM_MB_DATA58 >> 189 DQ58
5 MEM_MB_DATA59 >> 191 DQ59
5 MEM_MB_DATA60 >> 180 DQ60
5 MEM_MB_DATA61 >> 182 DQ61
5 MEM_MB_DATA62 >> 192 DQ62
5 MEM_MB_DATA63 >> 194 DQ63

5 MEM_MB_DQS0_N >> 11C DQS0#
5 MEM_MB_DQS1_N >> 29C DQS1#
5 MEM_MB_DQS2_N >> 49C DQS2#
5 MEM_MB_DQS3_N >> 68C DQS3#
5 MEM_MB_DQS4_N >> 129C DQS4#
5 MEM_MB_DQS5_N >> 146C DQS5#
5 MEM_MB_DQS6_N >> 167C DQS6#
5 MEM_MB_DQS7_N >> 186C DQS7#

5 MEM_MB_DQS0_P >> 13 DQS0
5 MEM_MB_DQS1_P >> 31 DQS1
5 MEM_MB_DQS2_P >> 51 DQS2
5 MEM_MB_DQS3_P >> 70 DQS3
5 MEM_MB_DQS4_P >> 131 DQS4
5 MEM_MB_DQS5_P >> 148 DQS5
5 MEM_MB_DQS6_P >> 169 DQS6
5 MEM_MB_DQS7_P >> 188 DQS7

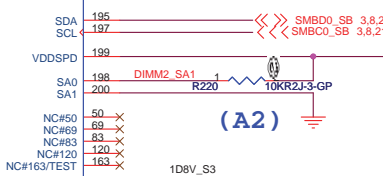
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5,10 MEM_MB0_ODT1 >> 119 OTD1



Place C2.2uF and 0.1uF < 500mils from DDR connector

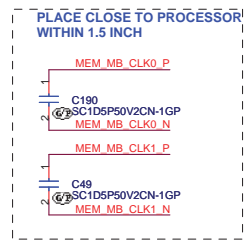
REVERSE TYPE

RAS# >> 108 A0
WE# >> 109 A1
CAS# >> 113 A2
CS0# >> 110 A3
CS1# >> 115 A4
CKE0 >> 79 A5
CKE1 >> 80 A6
CK0 >> 30 A7
CK0# >> 32 A8
CK1 >> 164 A9
CK1# >> 166 A10
DM0 >> 10 A11
DM1 >> 26 A12
DM2 >> 52 A13
DM3 >> 67 A14
DM4 >> 130 A15
DM5 >> 147 A16/BA2
DM6 >> 170 A17
DM7 >> 185 A18



VDD >> 81
VDD >> 82
VDD >> 87
VDD >> 88
VDD >> 95
VDD >> 96
VDD >> 103
VDD >> 104
VDD >> 111
VDD >> 112
VDD >> 117
VDD >> 118

VSS >> 3
VSS >> 8
VSS >> 9
VSS >> 12
VSS >> 15
VSS >> 18
VSS >> 21
VSS >> 24
VSS >> 27
VSS >> 28
VSS >> 33
VSS >> 34
VSS >> 40
VSS >> 41
VSS >> 42
VSS >> 47
VSS >> 48
VSS >> 53
VSS >> 54
VSS >> 59
VSS >> 60
VSS >> 65
VSS >> 66
VSS >> 71
VSS >> 72
VSS >> 77
VSS >> 78
VSS >> 121
VSS >> 122
VSS >> 127
VSS >> 128
VSS >> 132
VSS >> 133
VSS >> 138
VSS >> 139
VSS >> 144
VSS >> 145
VSS >> 149
VSS >> 150
VSS >> 155
VSS >> 156
VSS >> 161
VSS >> 162
VSS >> 165
VSS >> 168
VSS >> 171
VSS >> 172
VSS >> 177
VSS >> 178
VSS >> 183
VSS >> 184
VSS >> 187
VSS >> 190
VSS >> 193
VSS >> 196
GND >> 201
MH2 >> GP



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Title
DDR_SO-DIMM SKT_2

Size
Custom

Document Number
Big Bear 2A

Date
Monday, October 27, 2008

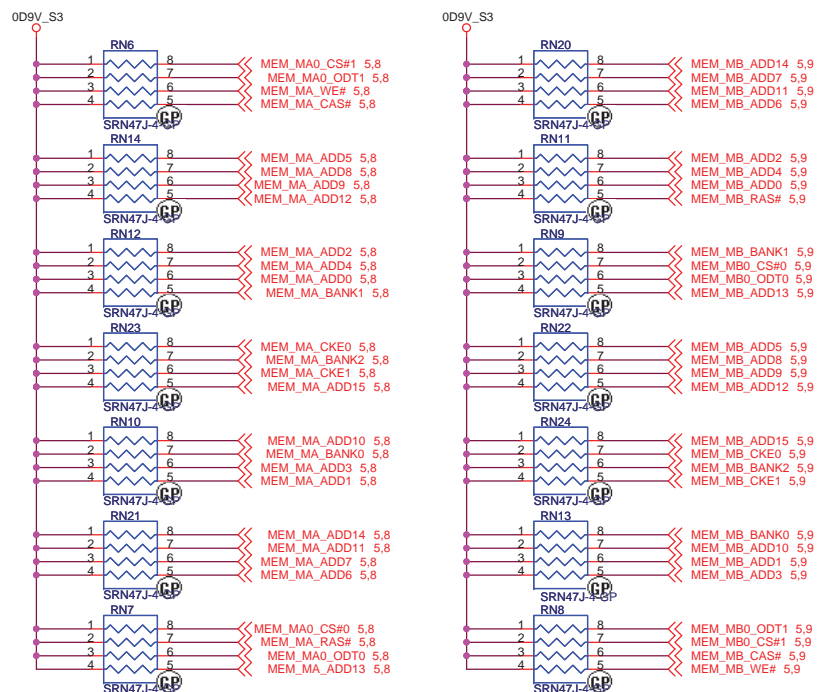
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PARALLEL TERMINATION

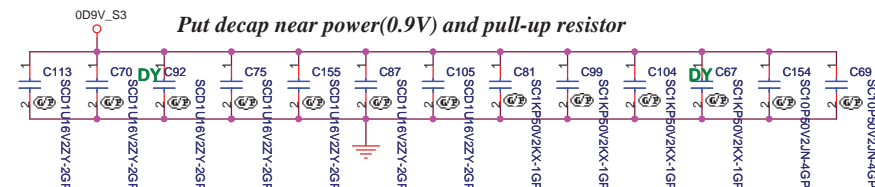
Put decap near power(0.9V) and pull-up resistor



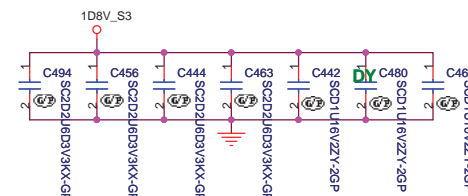
Do not share the Term resistor between the DDR address and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

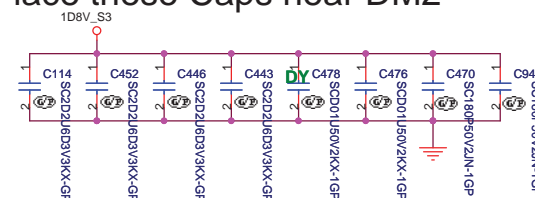


Place these Caps near DM1



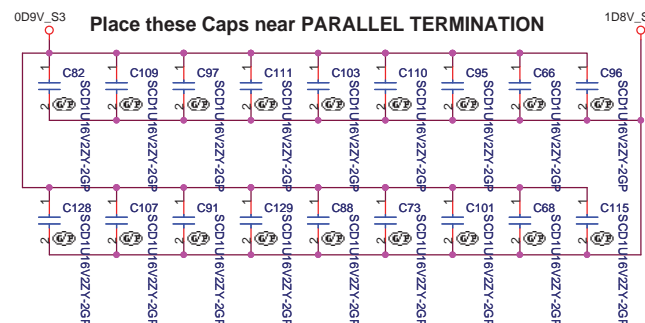
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to 0D9V S3

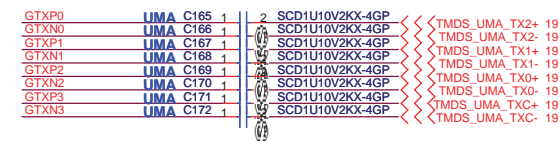
Place these Caps near PARALLEL TERMINATION



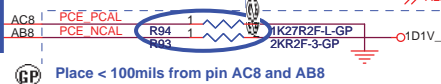
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
DDR DAMPING & TERMINATION			
Size	Document Number	Rev	
A3	Big Bear 2A	SA	
Date:	Monday, October 27, 2008	Sheet	10 of 55

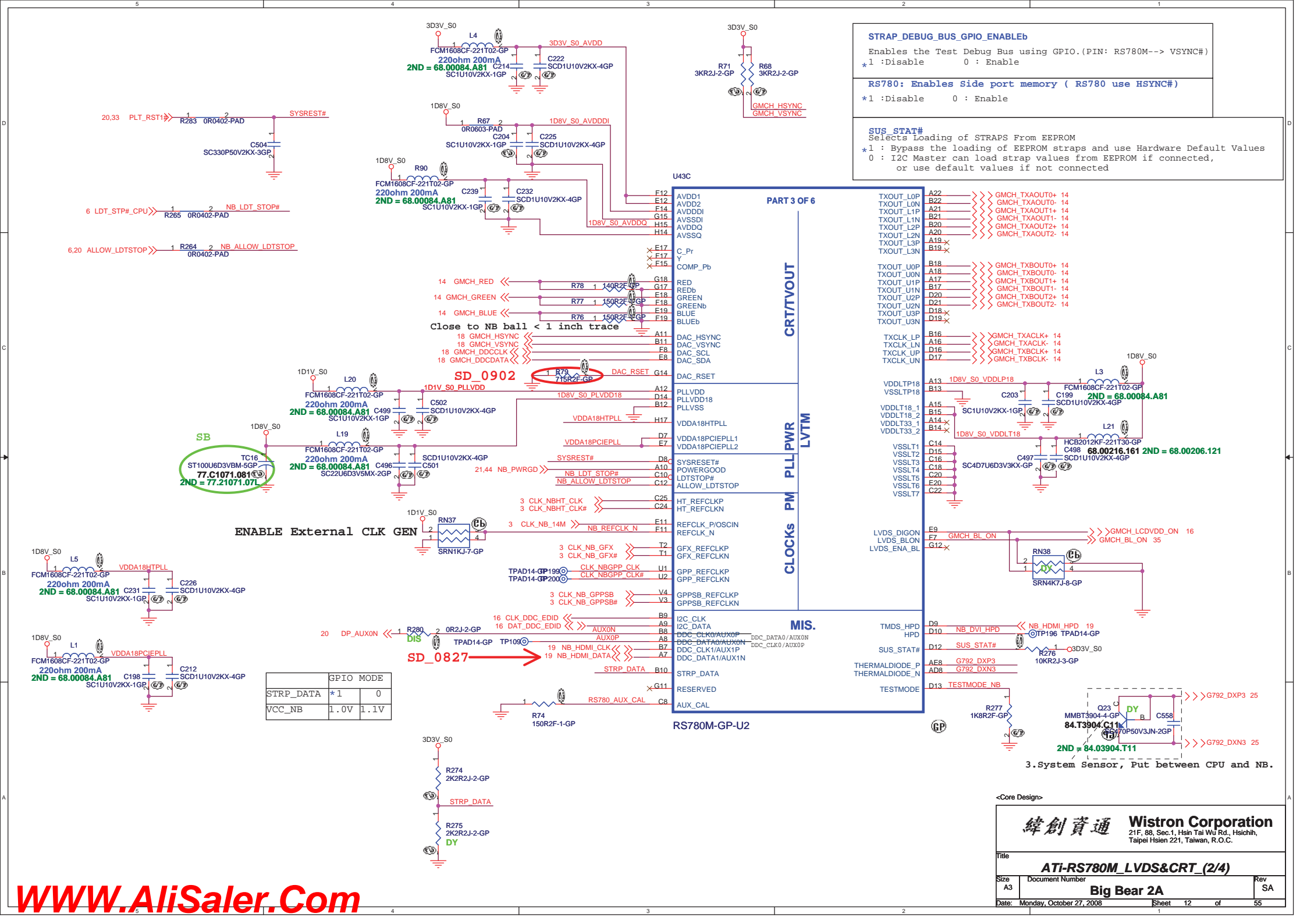


DP0	GFX_TX0, TX1, TX2, TX3, AUX0, HPD0
DP1	GFX_TX4, TX5, TX6, TX7, AUX1, HPD1



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Title			
ATI-RS780M_HT LINK&PCle(1/3)			
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STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable

SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

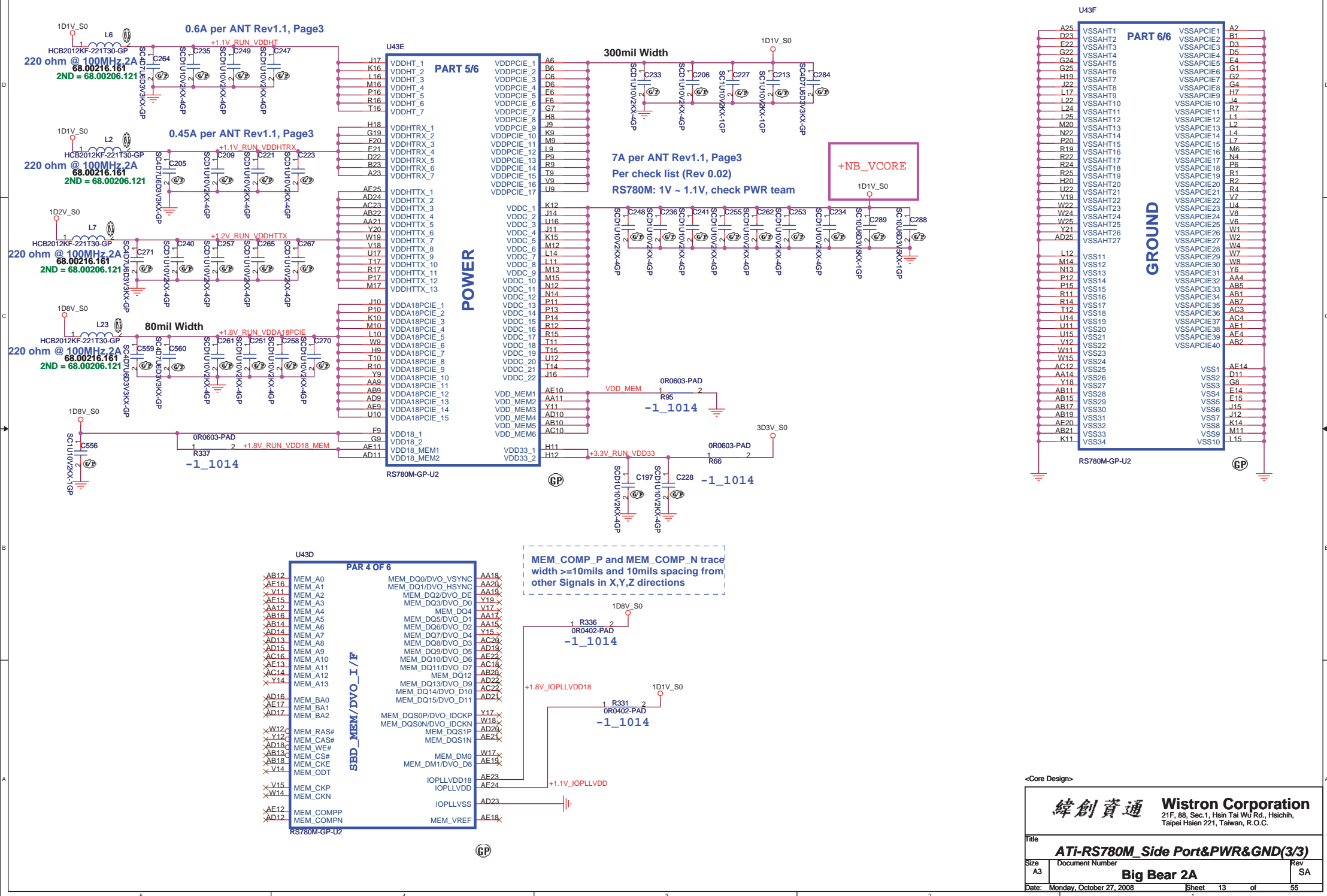
	GPIO MODE
STRP_DATA	*1 0
VCC_NB	1.0V 1.1V

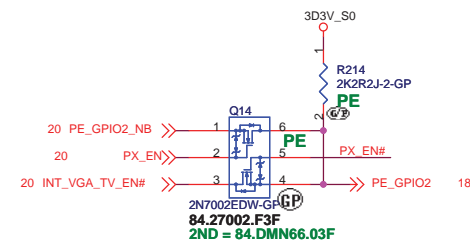
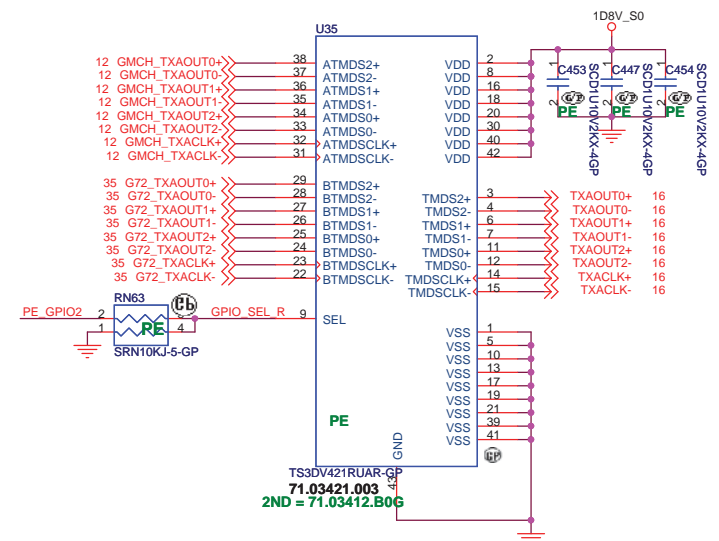
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Title: **ATI-RS780M_LVDS&CRT (2/4)**

Size A3	Document Number	Rev SA
Big Bear 2A		
Date: Monday, October 27, 2008	Sheet 12 of 55	

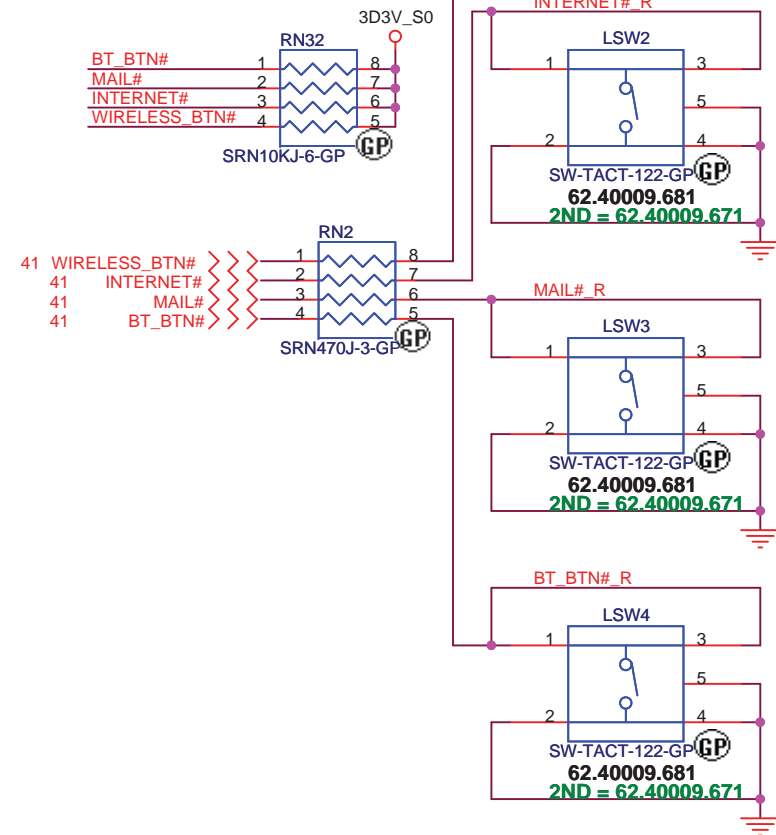
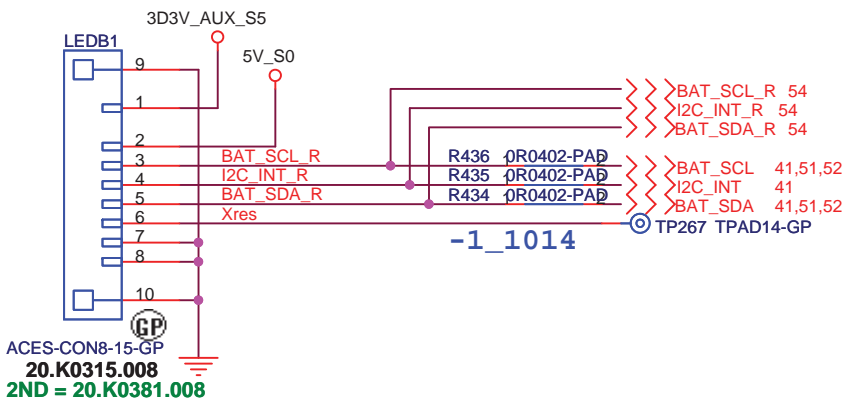
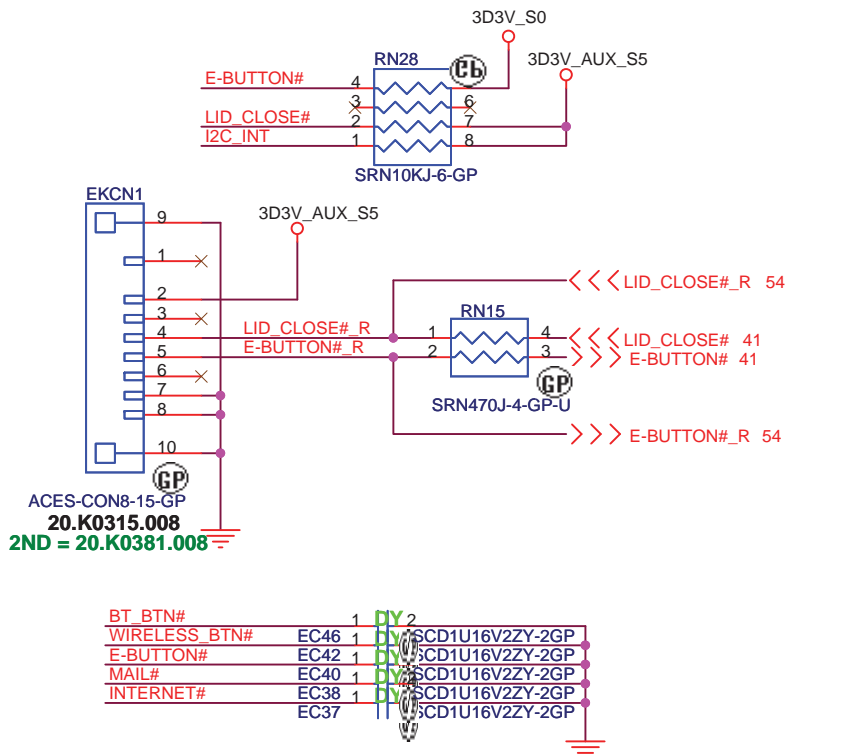


[illegible]

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LAUNCH



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LAUNCH & LID

Size
A4

Document Number

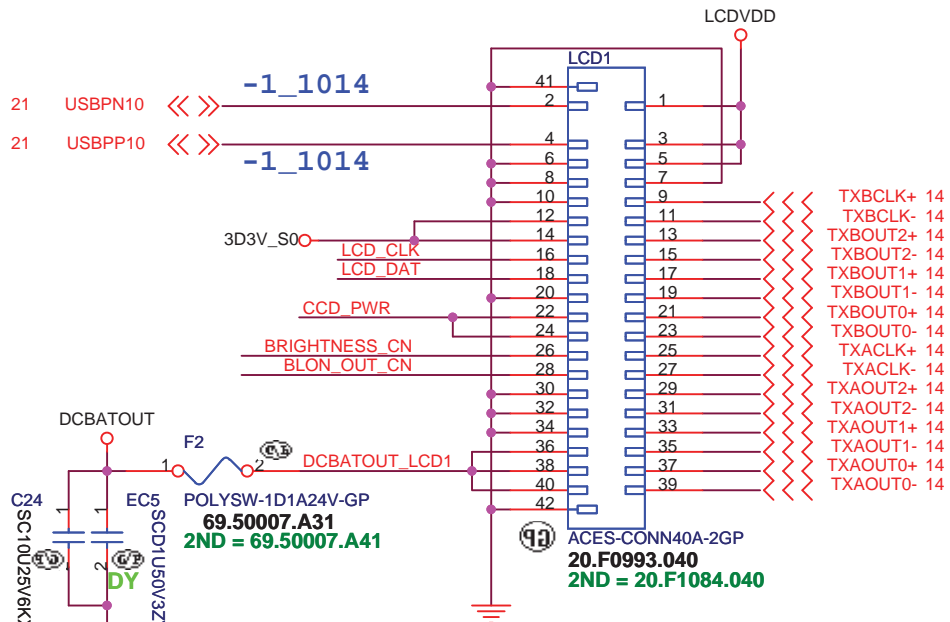
Big Bear 2A

Rev
SC

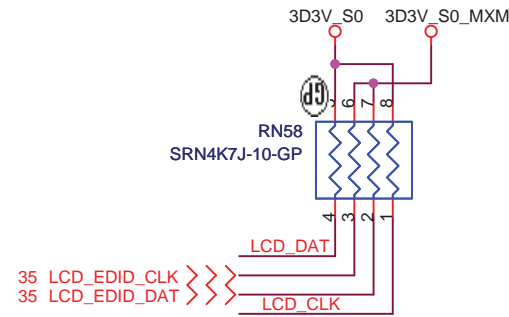
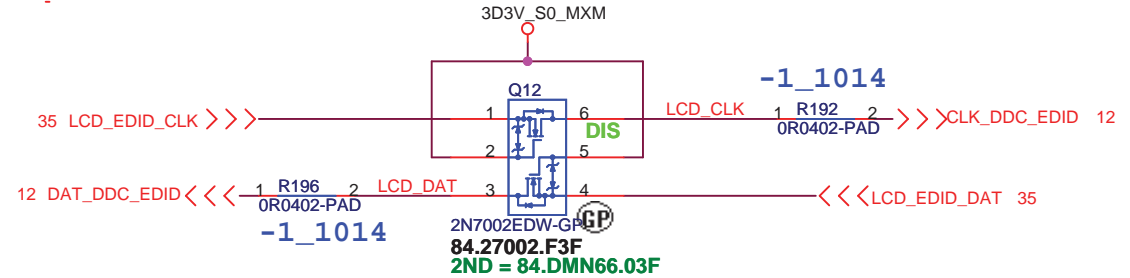
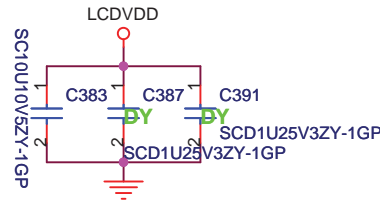
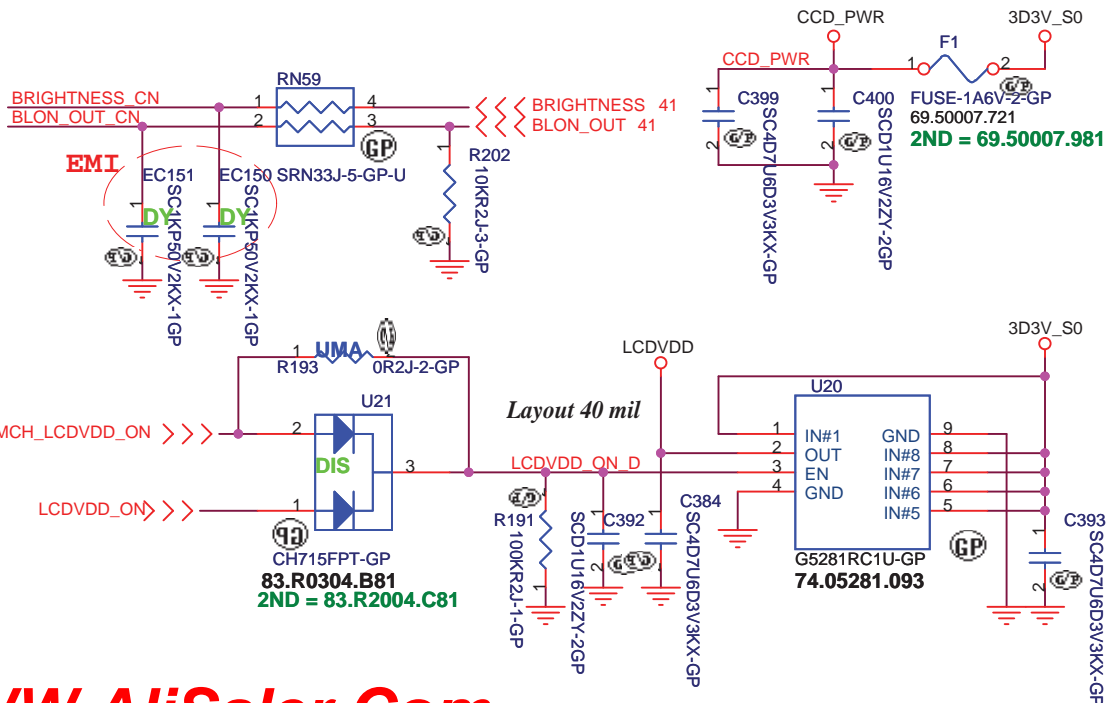
Date: Monday, October 27, 2008

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LCD/INVERTER/CCD CONN



SD_0901:Change "LCD1" Pin 7, 8, 10 to GND.



<Core Design>

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Title

LCD CONN

Size
A4

Document Number

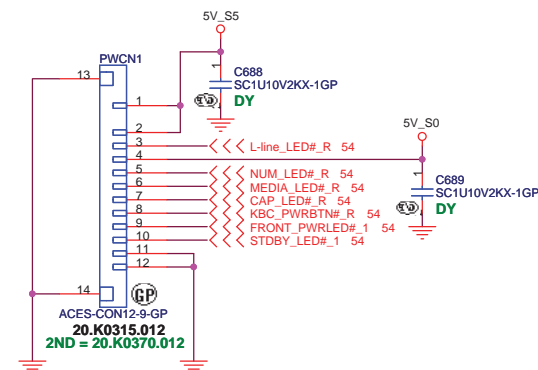
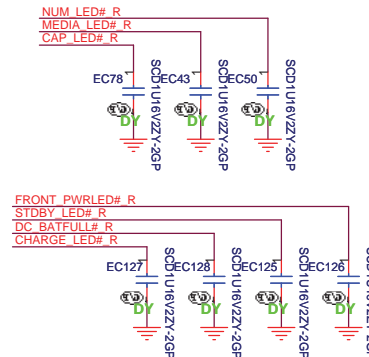
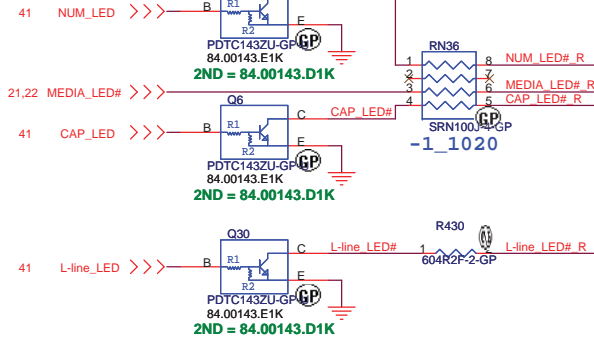
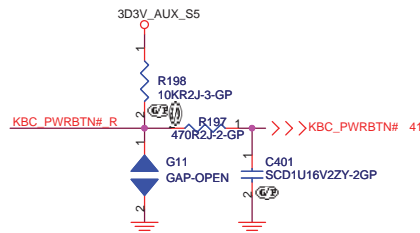
Big Bear 2A

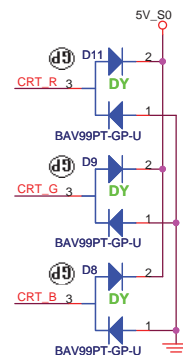
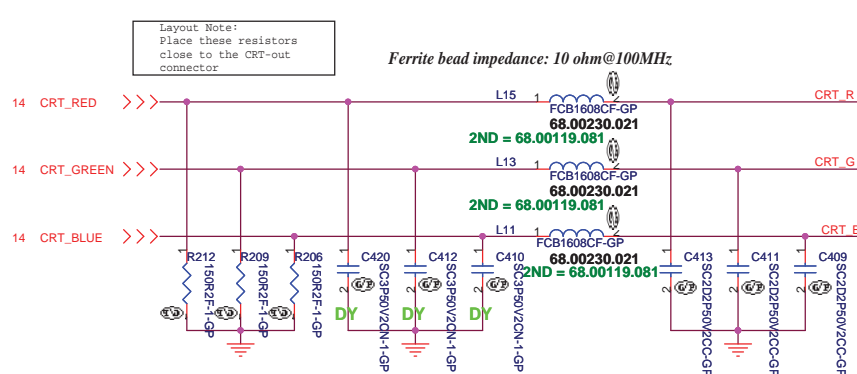
Rev
SC

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LED



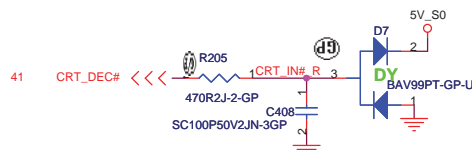
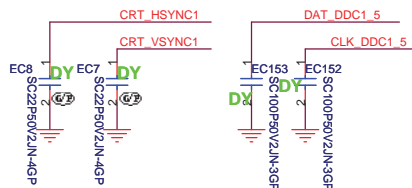
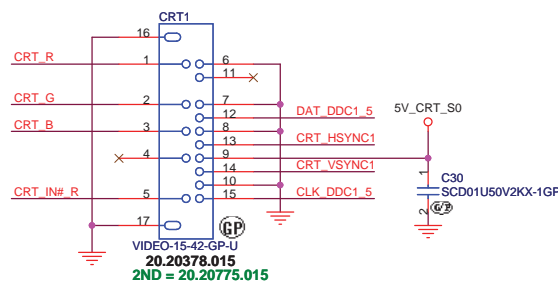
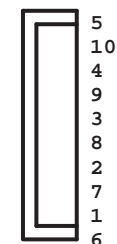


Change C409; C411, C413 to 1.5pF (78.1R574.1FL) in UMA

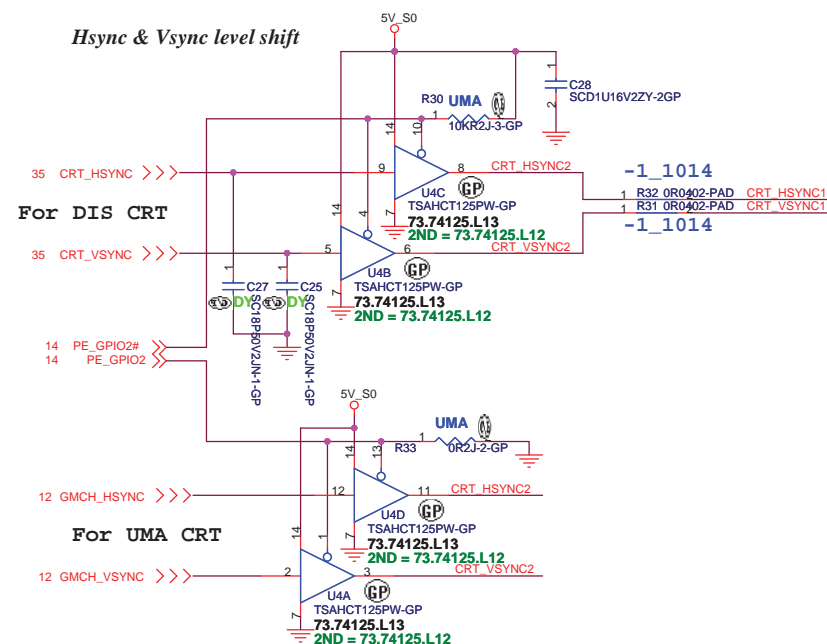
Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, then CRT CONN.

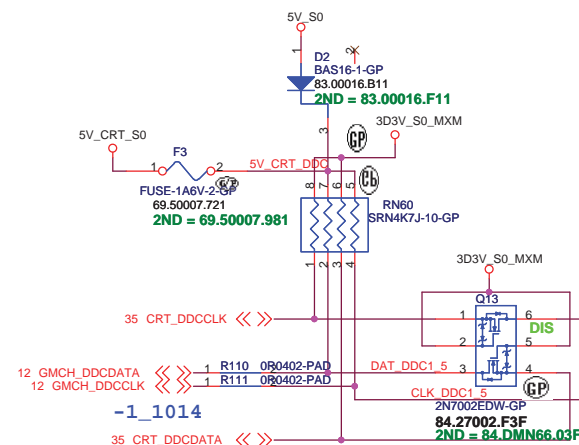
CRT I/F & CONNECTOR



Hsync & Vsync level shift



DDC_CLK & DATA level shift

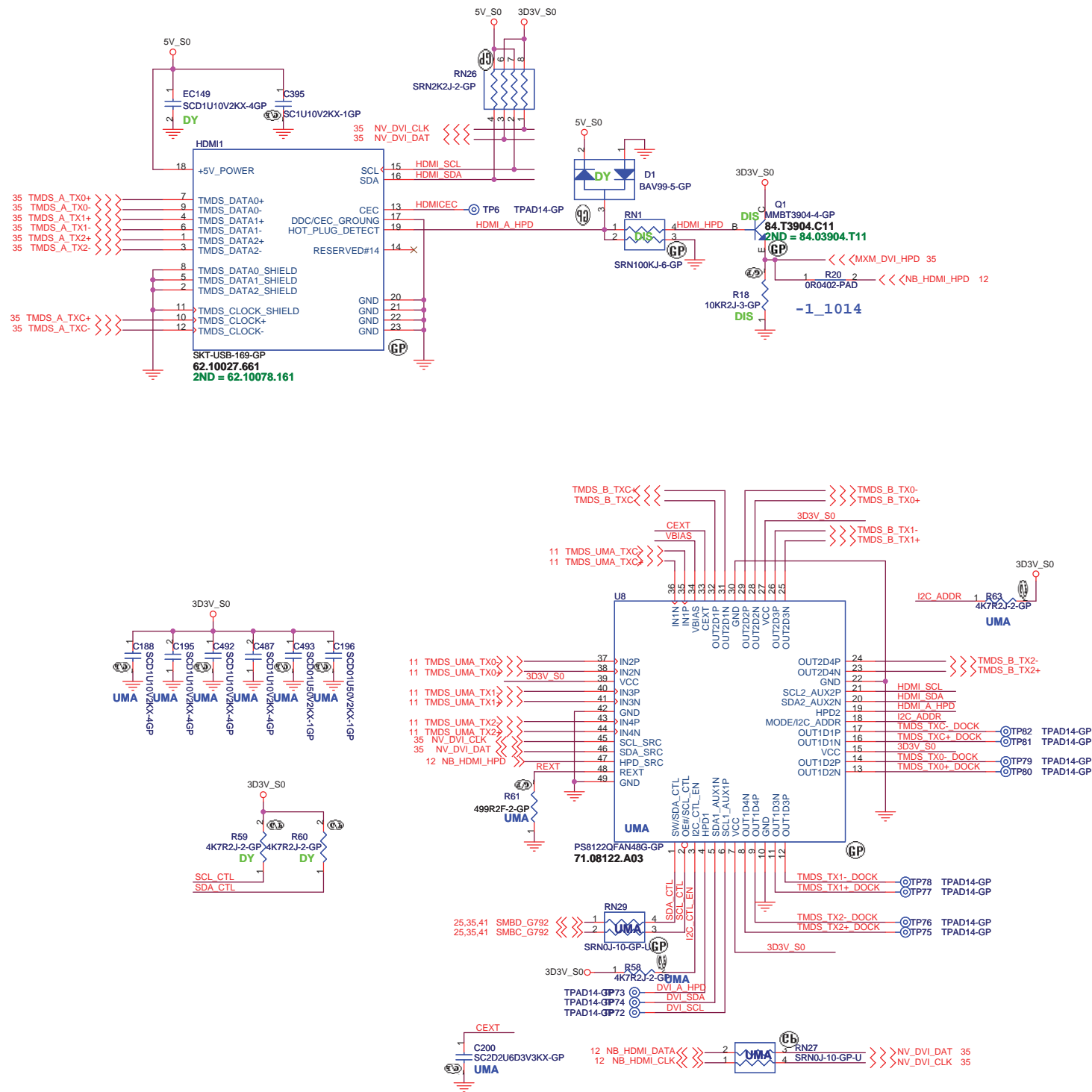


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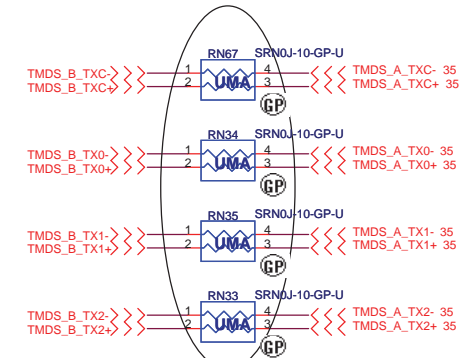
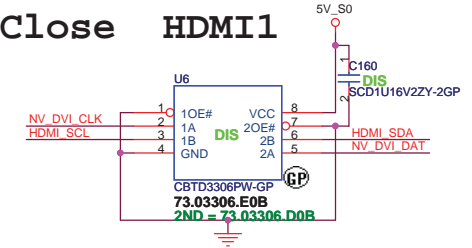
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Taipei Hsien 221, Taiwan, R.O.C.

Title		CRT Connector	
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HDMI SM BUS LEVEL shifter



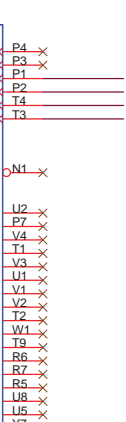
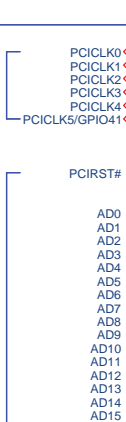
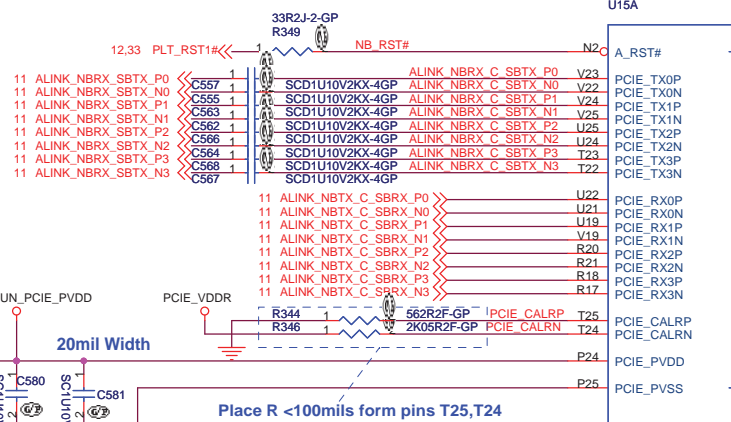
Close HDMI1



Place near MXM connector

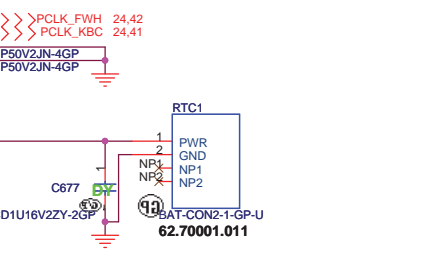
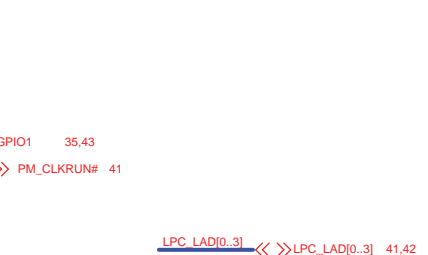
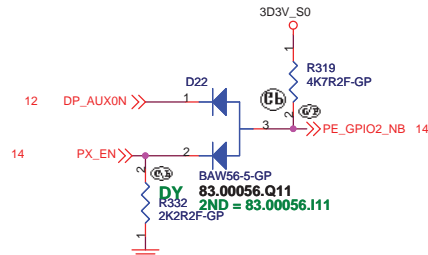
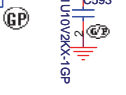
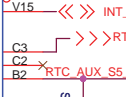
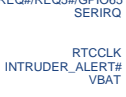
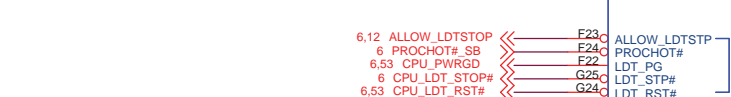
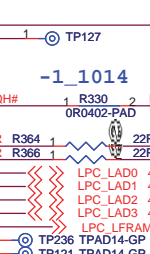
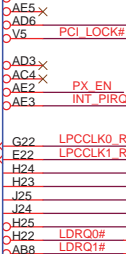
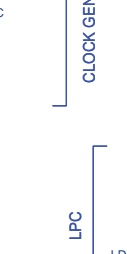
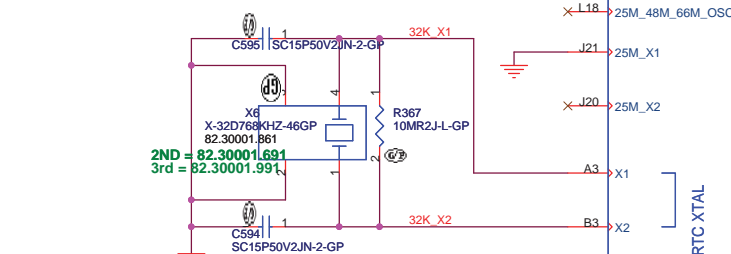
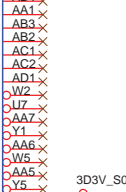
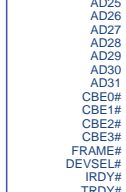
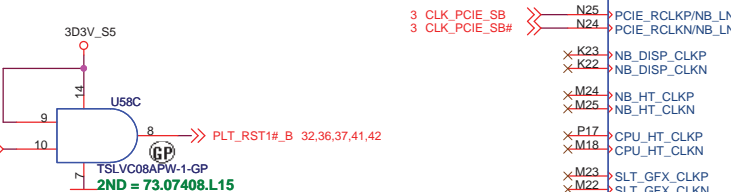
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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HDMI CONNECTOR			
Size	Document Number	Rev	
A3	Big Bear 2A	SD	
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POWER EXPRESS SUPPORT

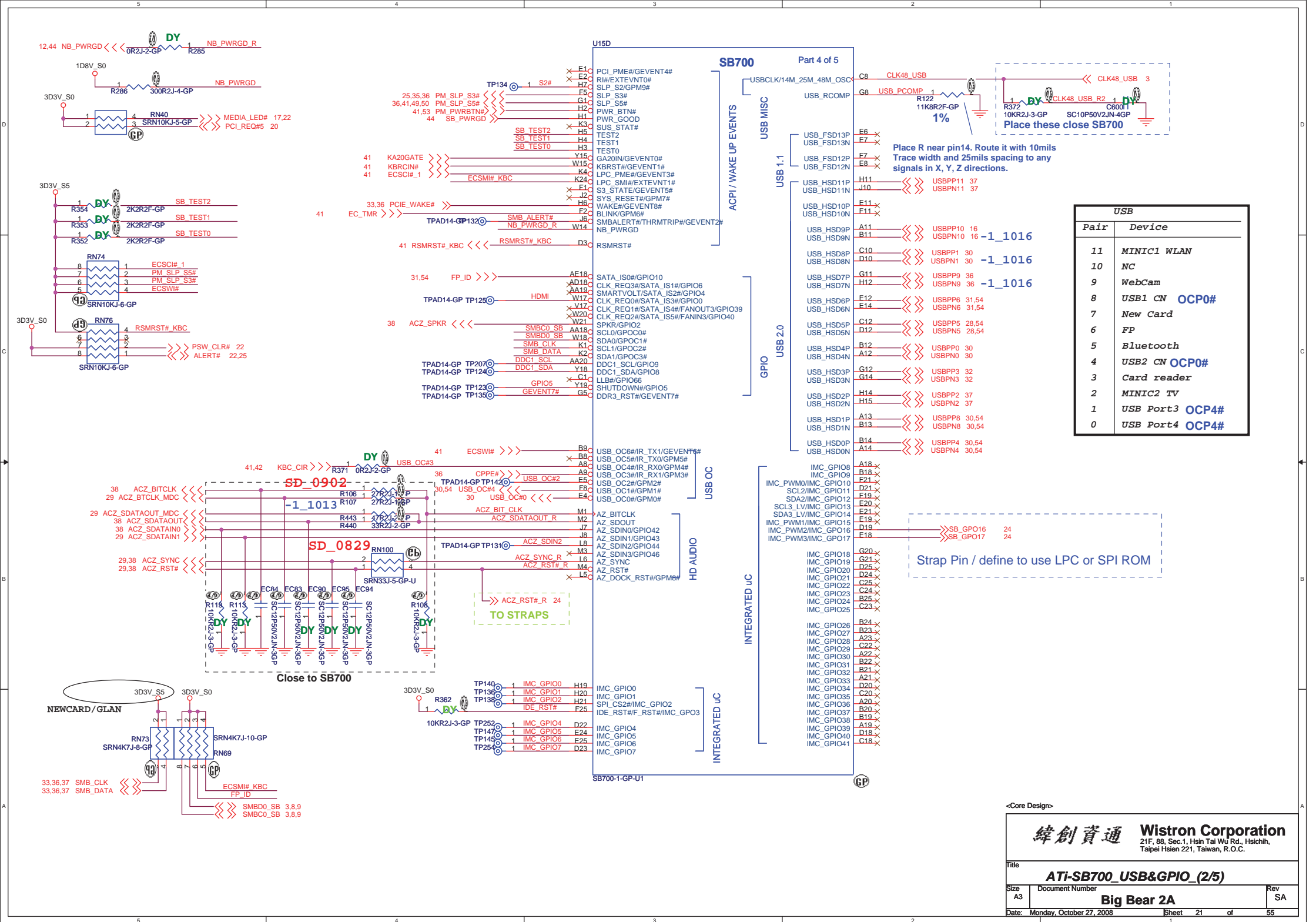
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH
TMD5_HPD0 MXM HOT PLUG



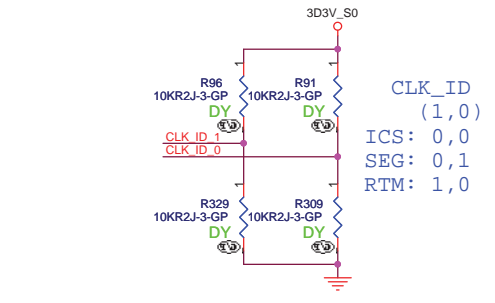
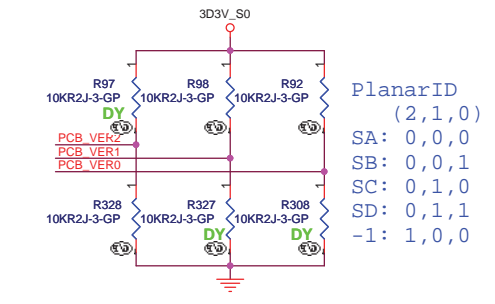
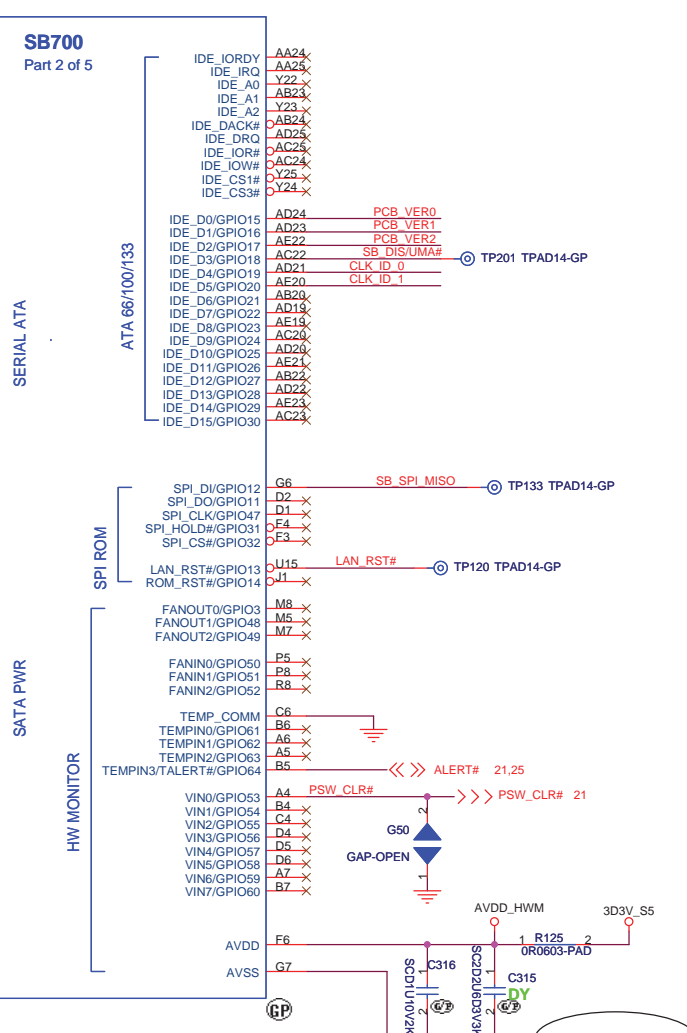
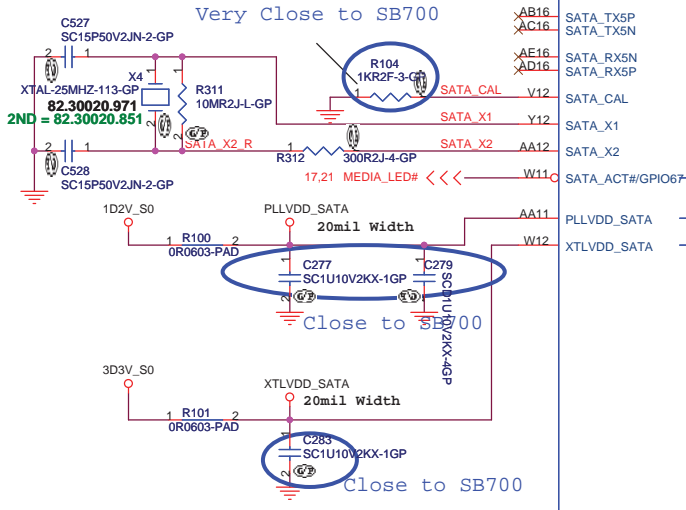
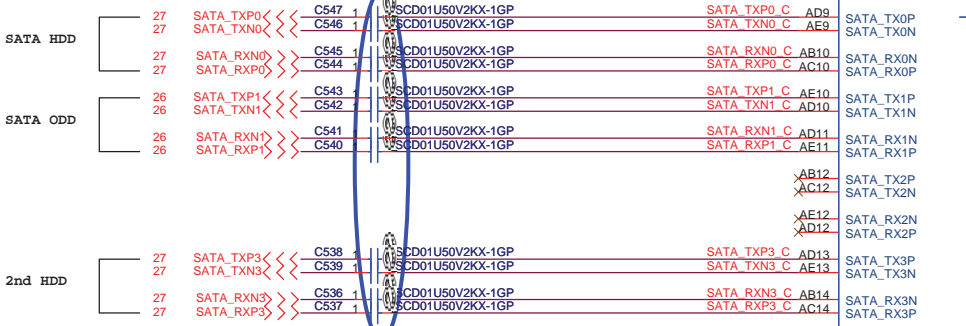
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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			ATI-SB700_PCIE&PCI_(1/5)
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A3		SA	
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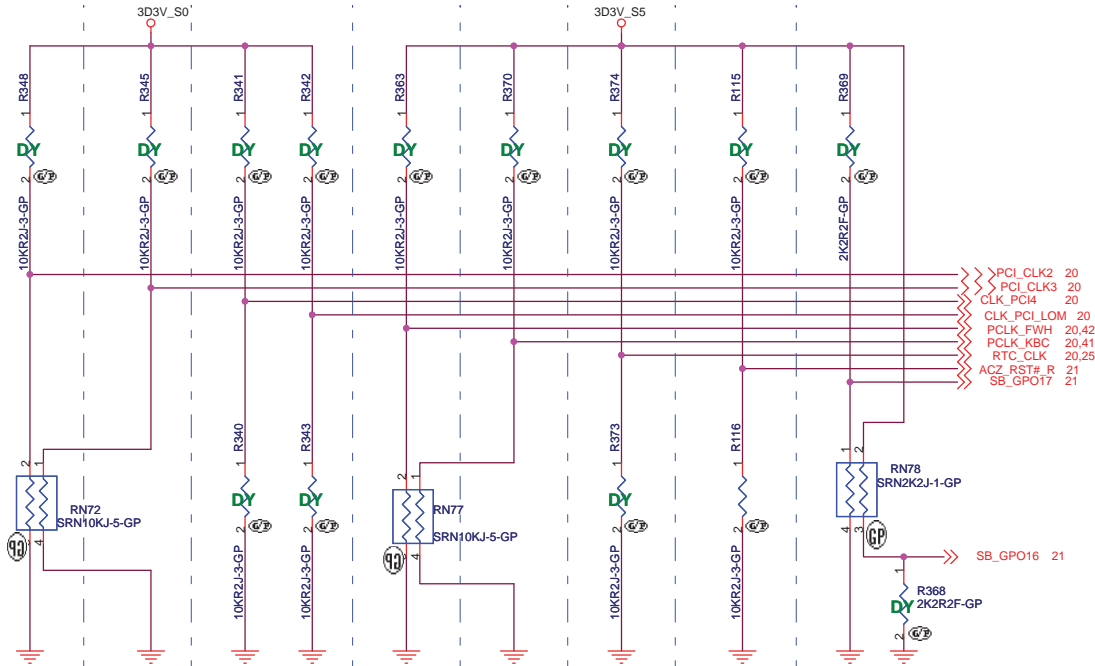


PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700



REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



DEBUG STRAPS

	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17, SB_GPO16
PULL HIGH	WatchDog (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

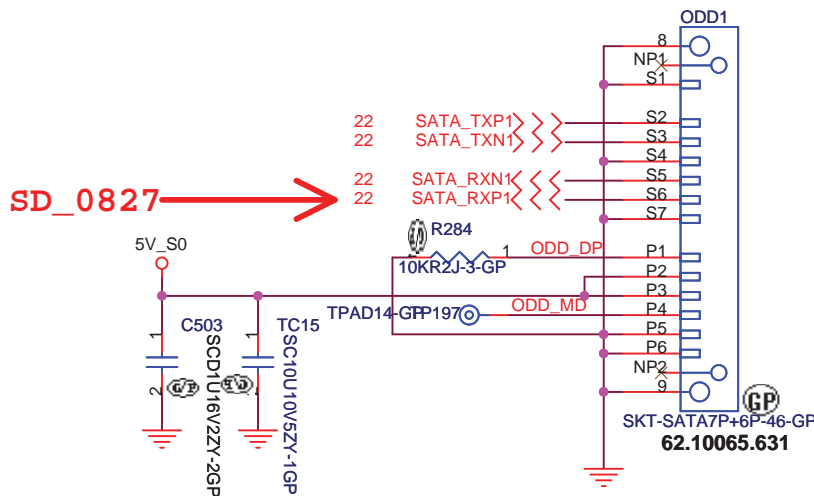
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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

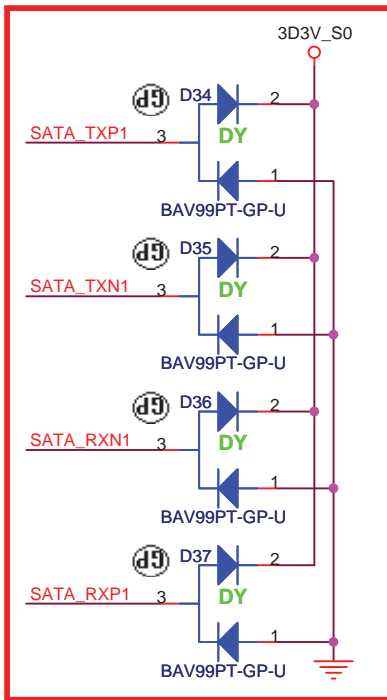
Title		ATI-SB700 STRAPPING (5/5)	
Size	Document Number	Rev	
A3		SA	
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Big Bear 2A

ODD Connector



SD_0828

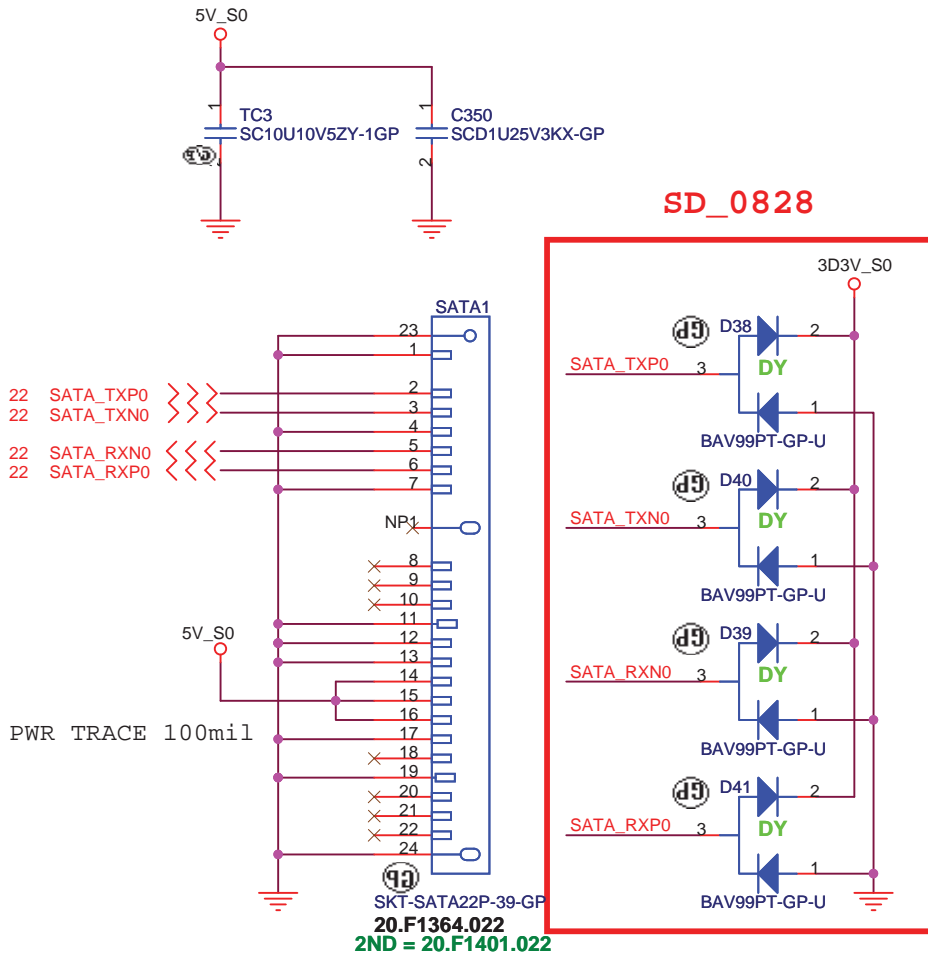


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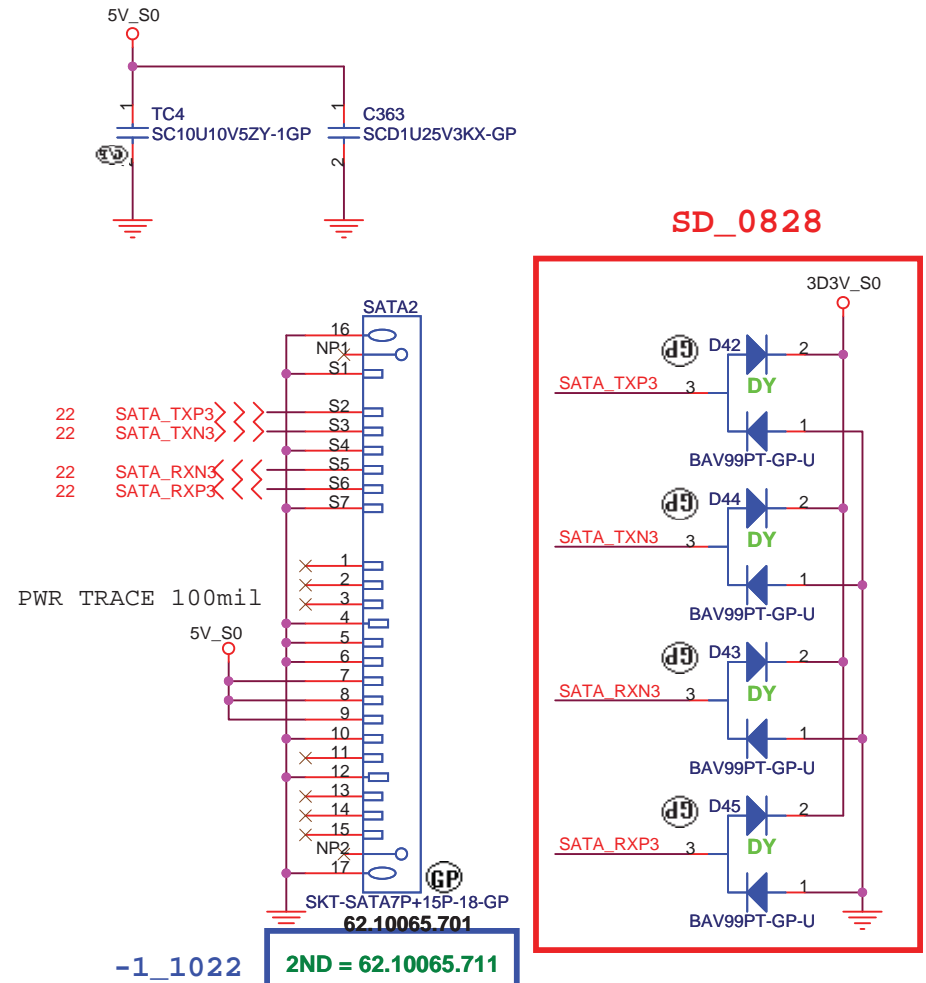
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
CDROM		
Size	Document Number	Rev
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SATA HDD Connector



2ND SATA HDD Connector



<Core Design>

緯創資通

Wistron Corporation
215 22 2nd Fl. Hsinchu City, Taiwan

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

HDD

Size	Document Number
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A4

Big Bear 2A

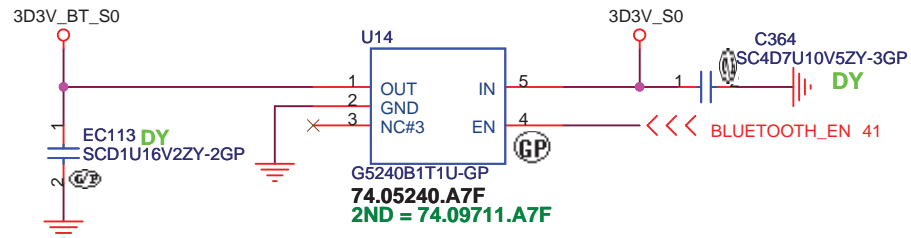
Rev

SD

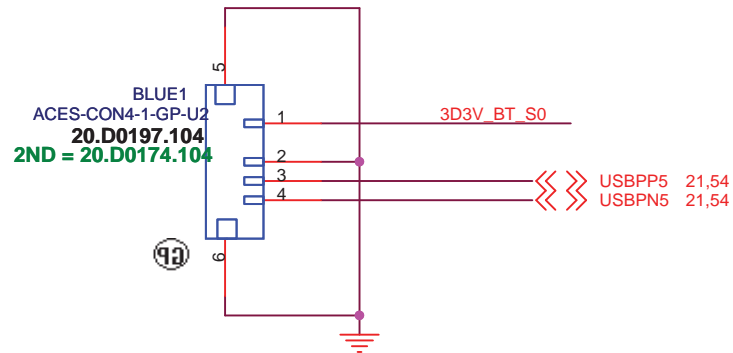
Date: Monday, October 27, 2008

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BLUETOOTH MODULE



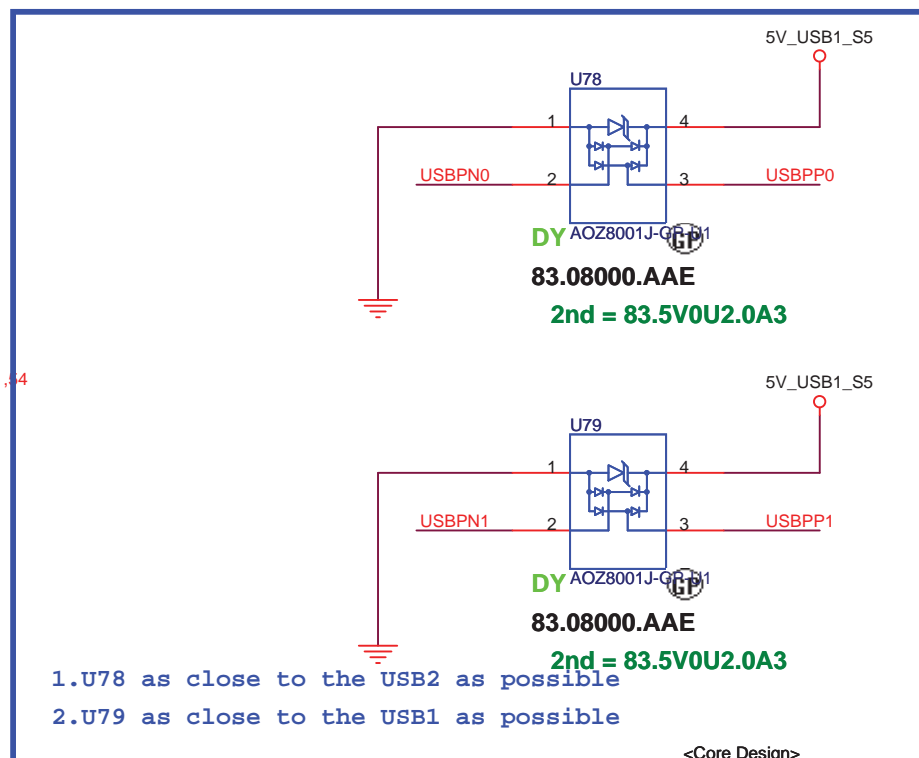
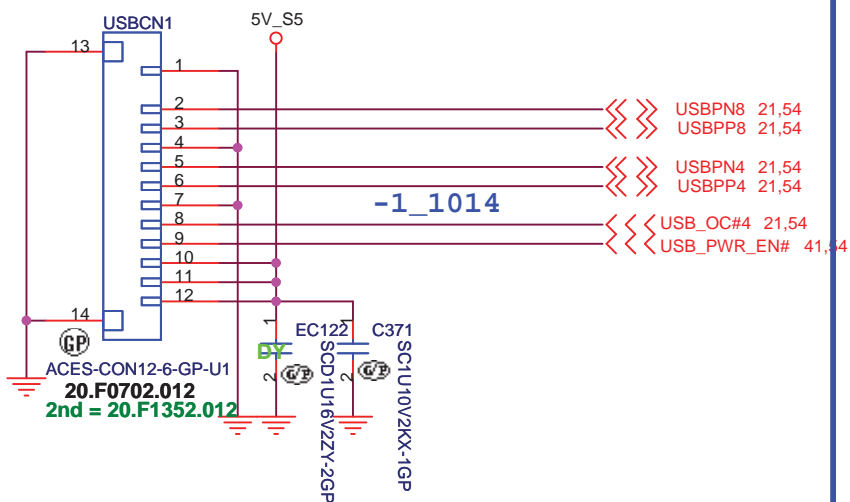
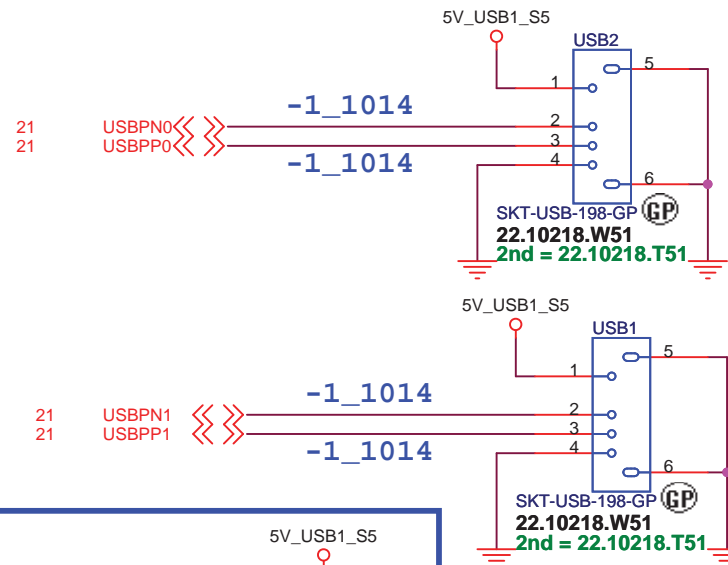
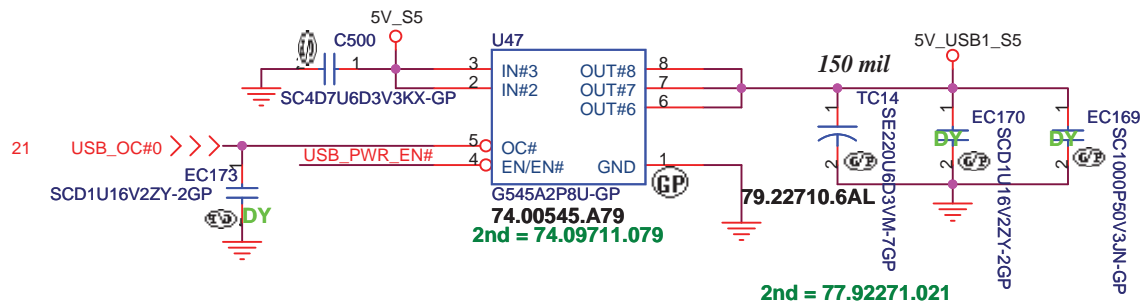
EC40 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BLUETOOTH		
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ESD Protection

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

USB

Size

A4

Document Number

Big Bear 2A

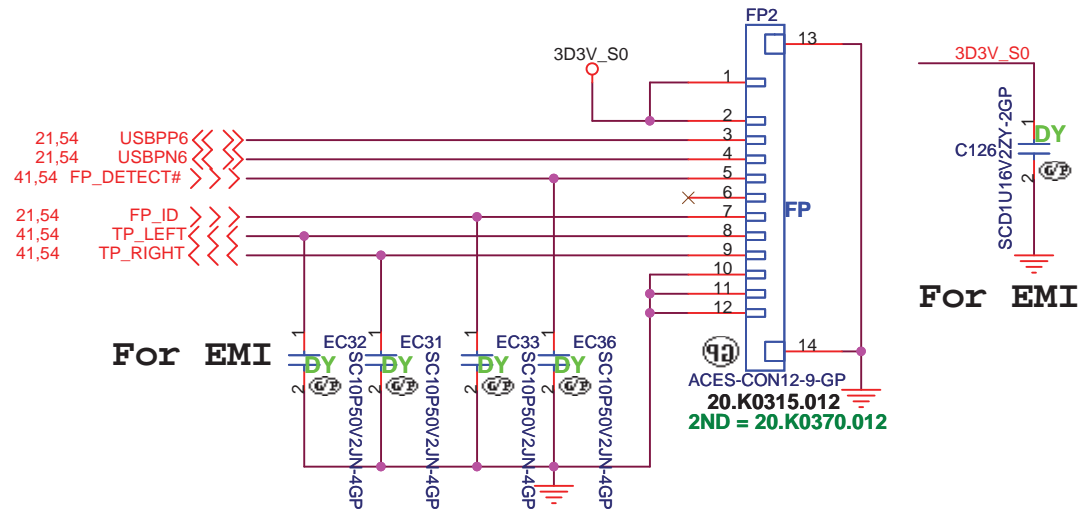
Rev

SB

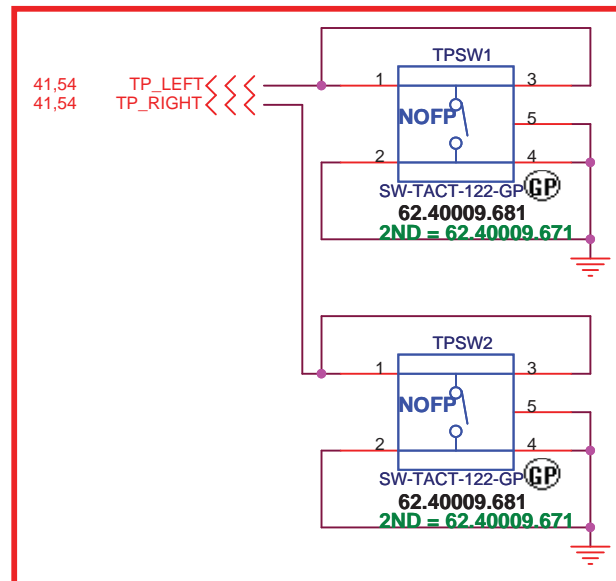
Date: Monday, October 27, 2008

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Finger printer



SD_0903



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title

Finger Printer

Size

Document Number

A4

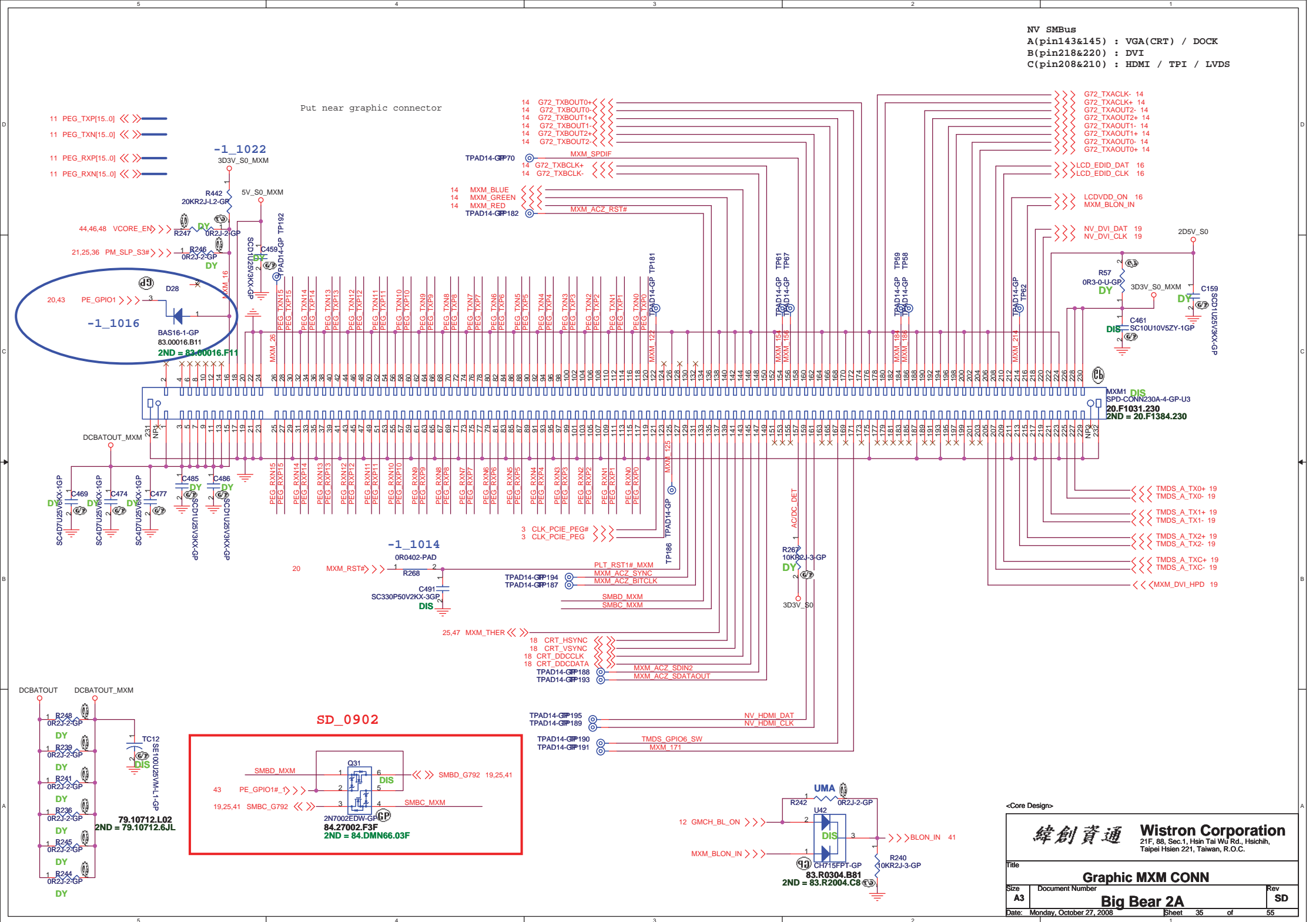
Big Bear 2A

Rev

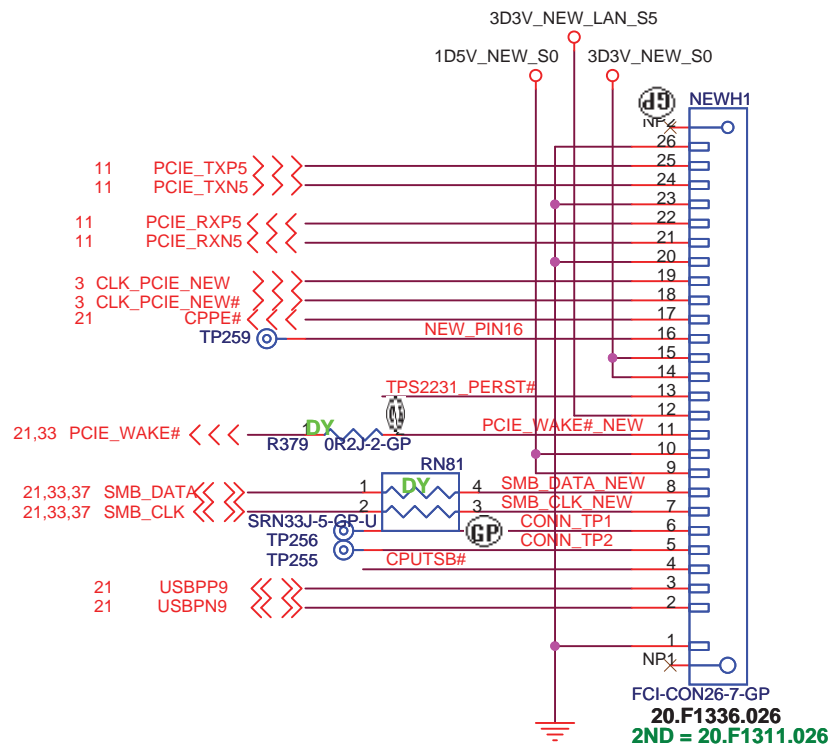
SD

Date: Monday, October 27, 2008

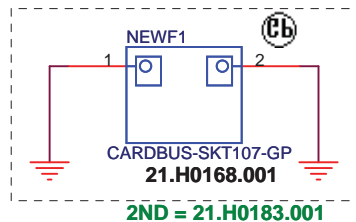
Sheet 31 of 55



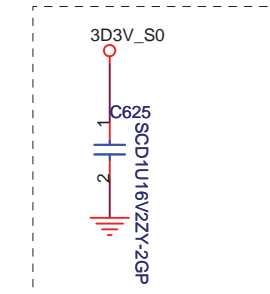
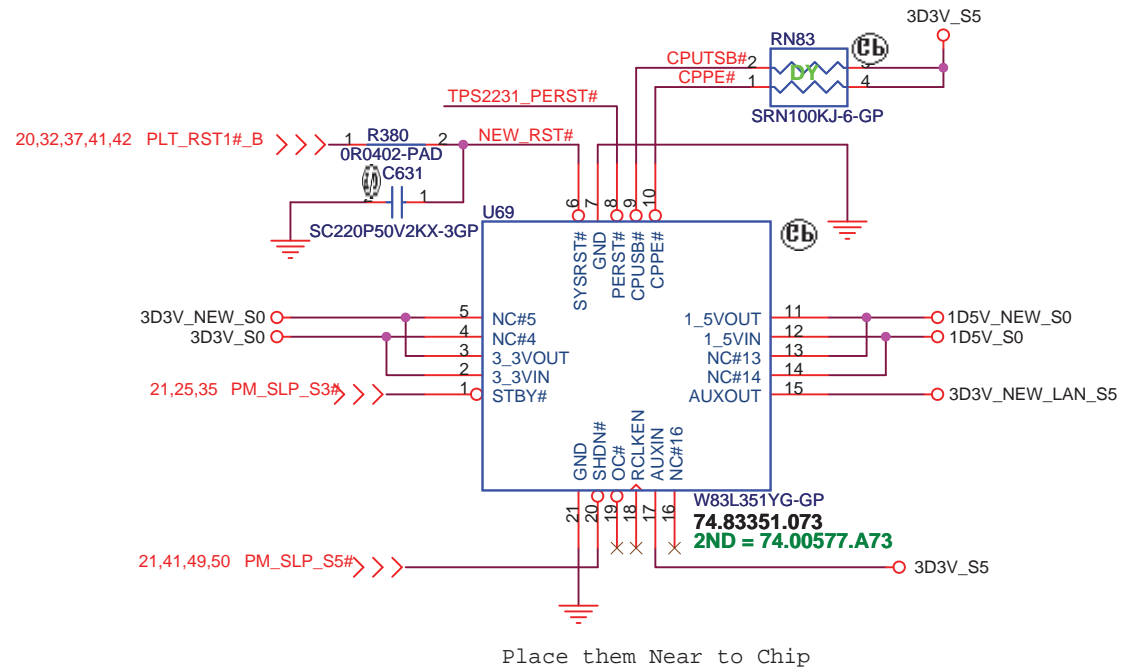
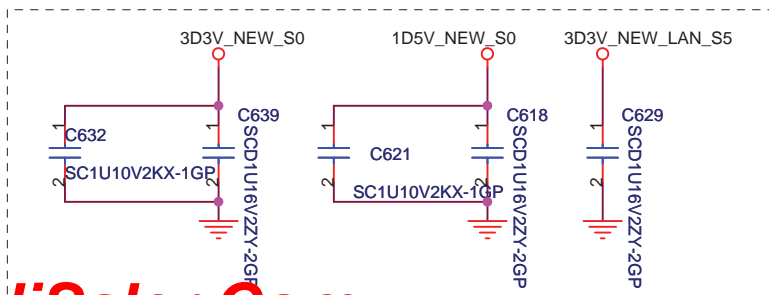
NEWCARD Connector



TOP VIEW



Place them Near to Connector



<Core Design>

緯創資通

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Title

NEW CARD

Size

Document Number

A4

Big Bear 2A

Rev

SC

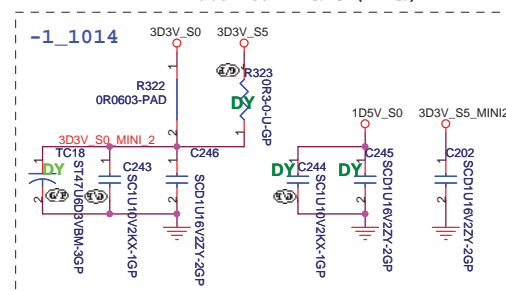
Date: Monday, October 27, 2008

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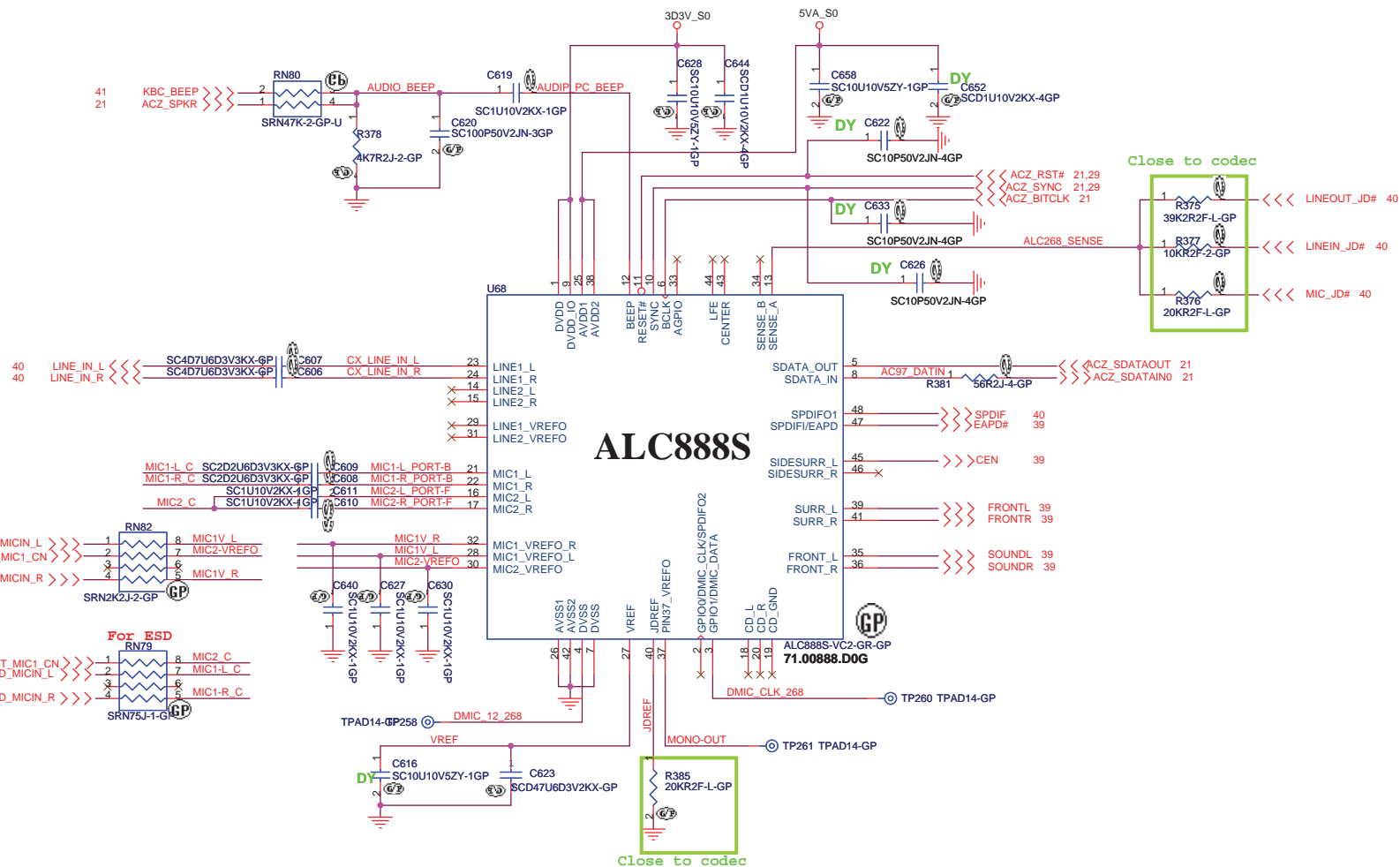
Mini Card Connector(TV) UPPER SLOT
Mini Card Connector(WLAN) LOWER SLOT



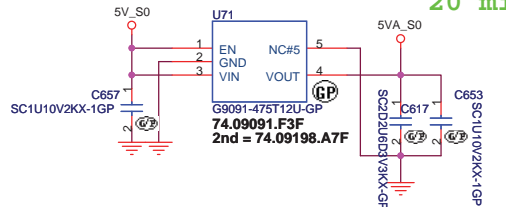
Place near MINIC1(WLAN)



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Title			
		Mini Card	
Size A3	Document Number		Rev SA
Date: Monday, October 27, 2008		Big Bear 2A	
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POWER GENERATE *Layout* 20 mil



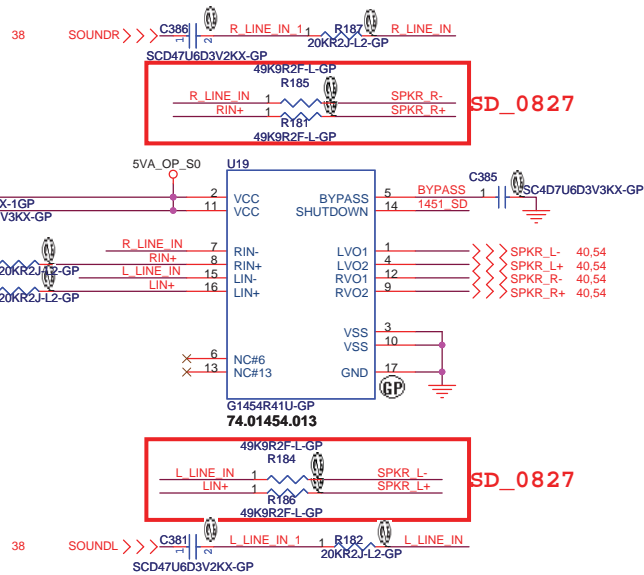
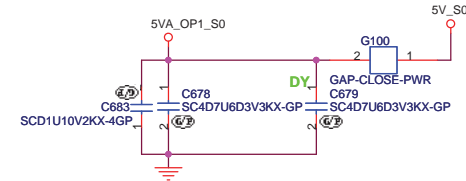
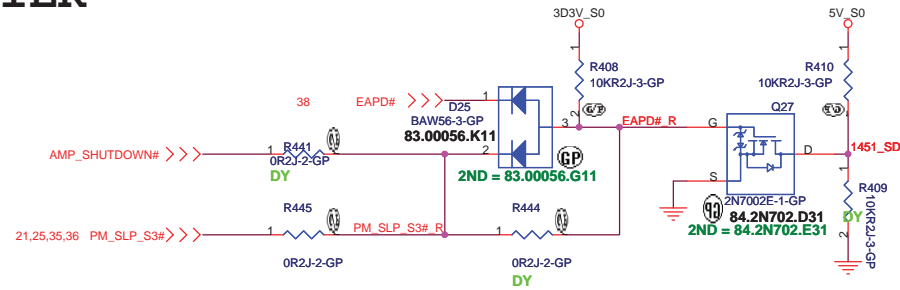
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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

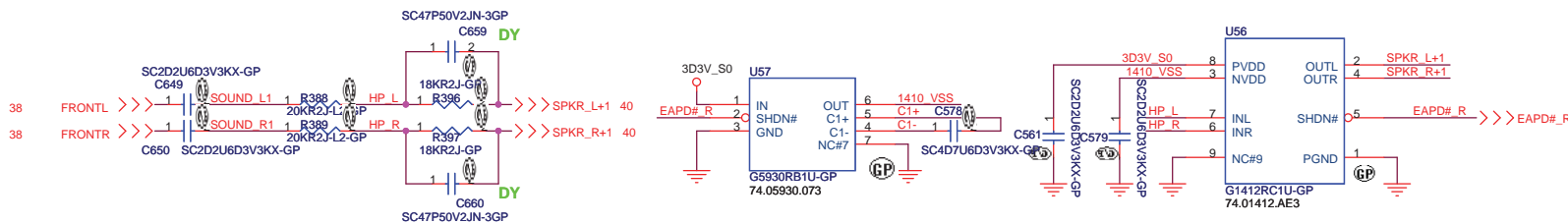
Title **Azalia codec ALC268**

Size **A3** Document Number **Big Bear 2A** Rev **SA**

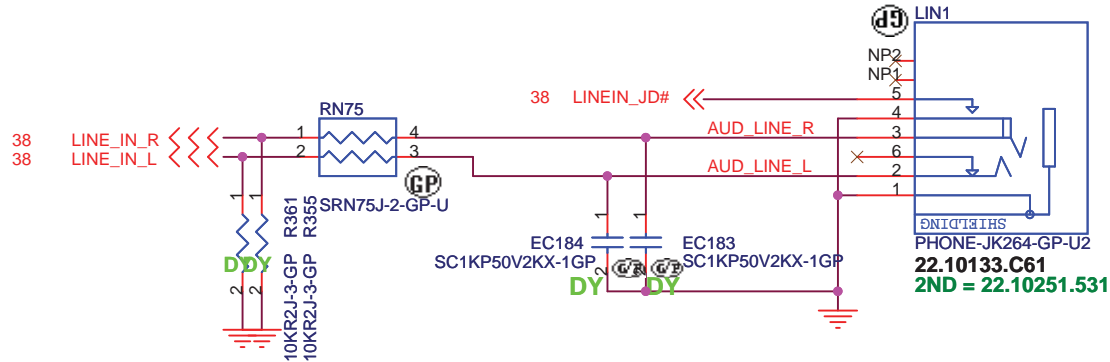
Date: Monday, October 27, 2008 Sheet 38 of 55

[illegible]

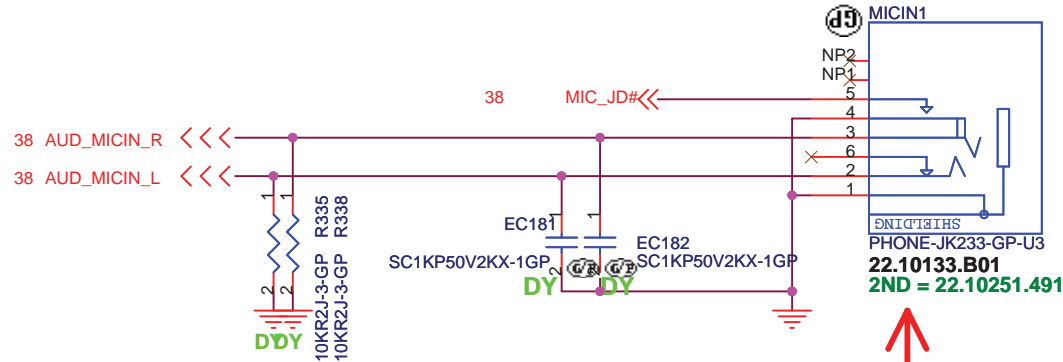
KBC_MUTE_GPIO8



LINE IN

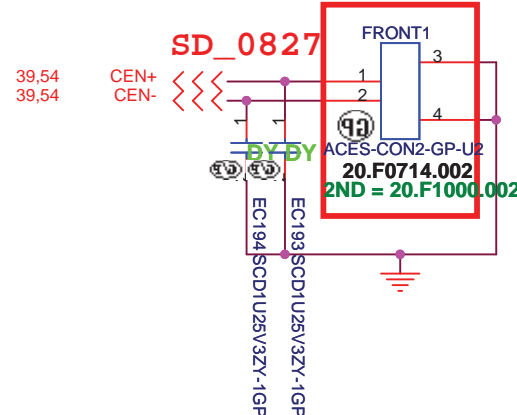


MIC IN

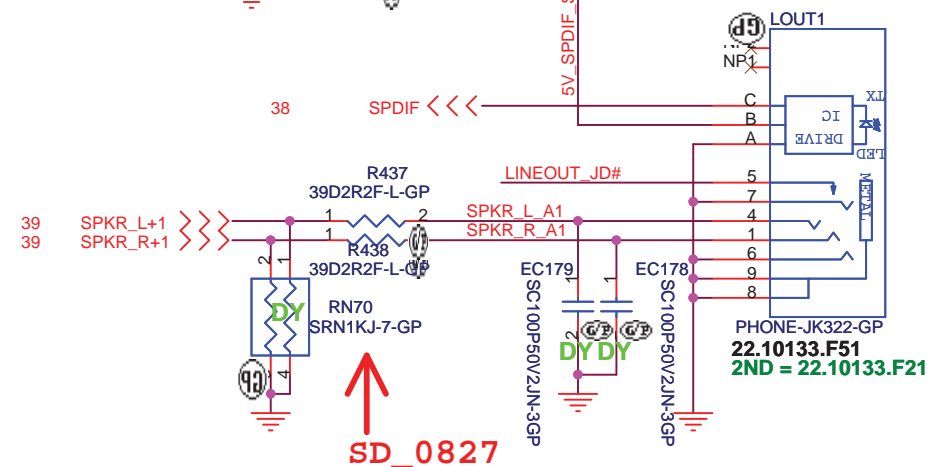
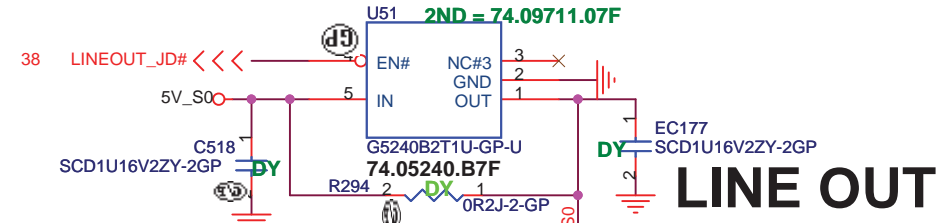
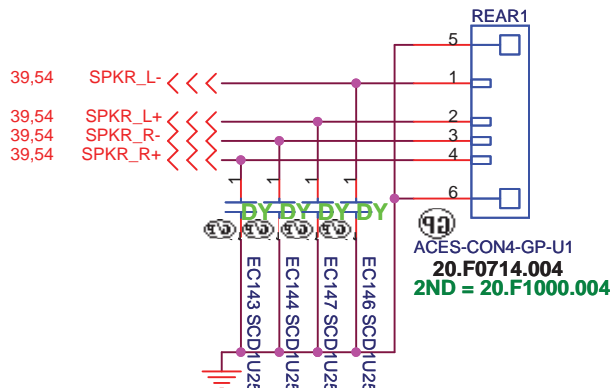


SD_0912 change 2nd

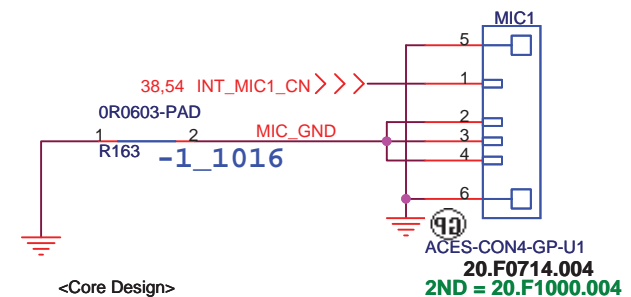
SUBWOOFER



REAR Speaker



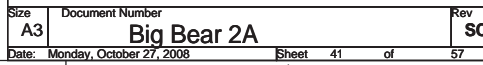
INT. MIC



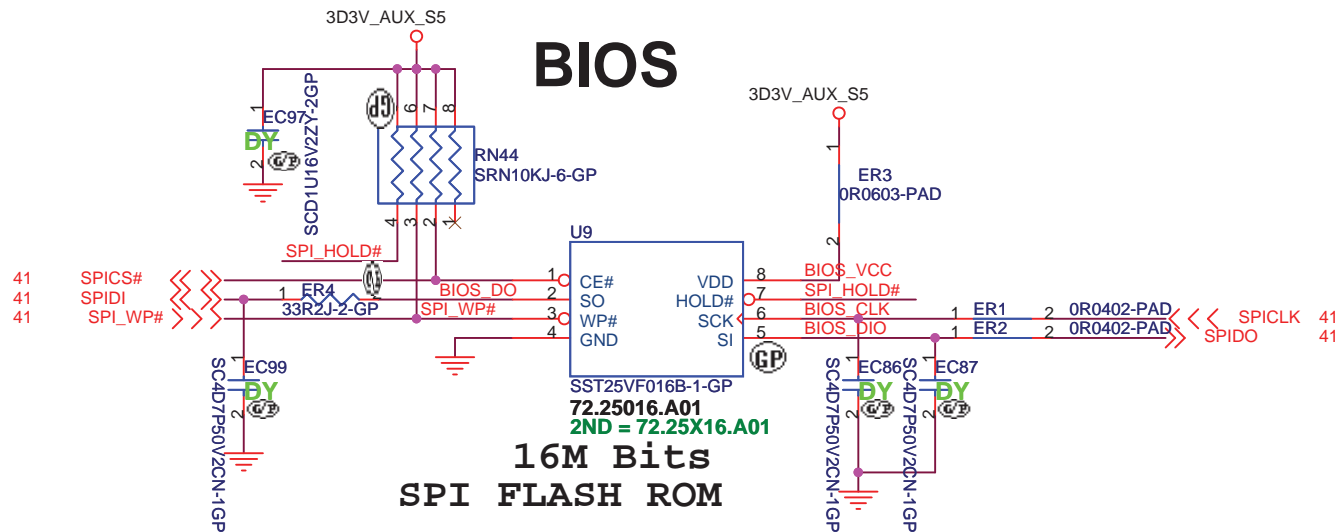
緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

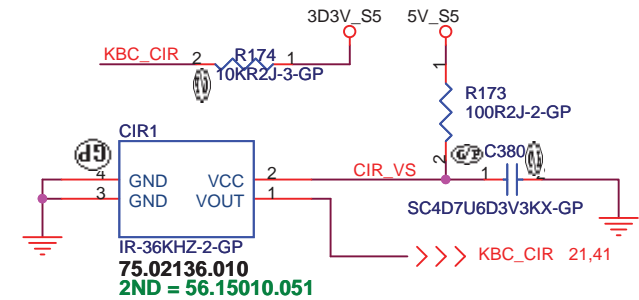
Title			
AUDIO JACK			
Size	Document Number		Rev
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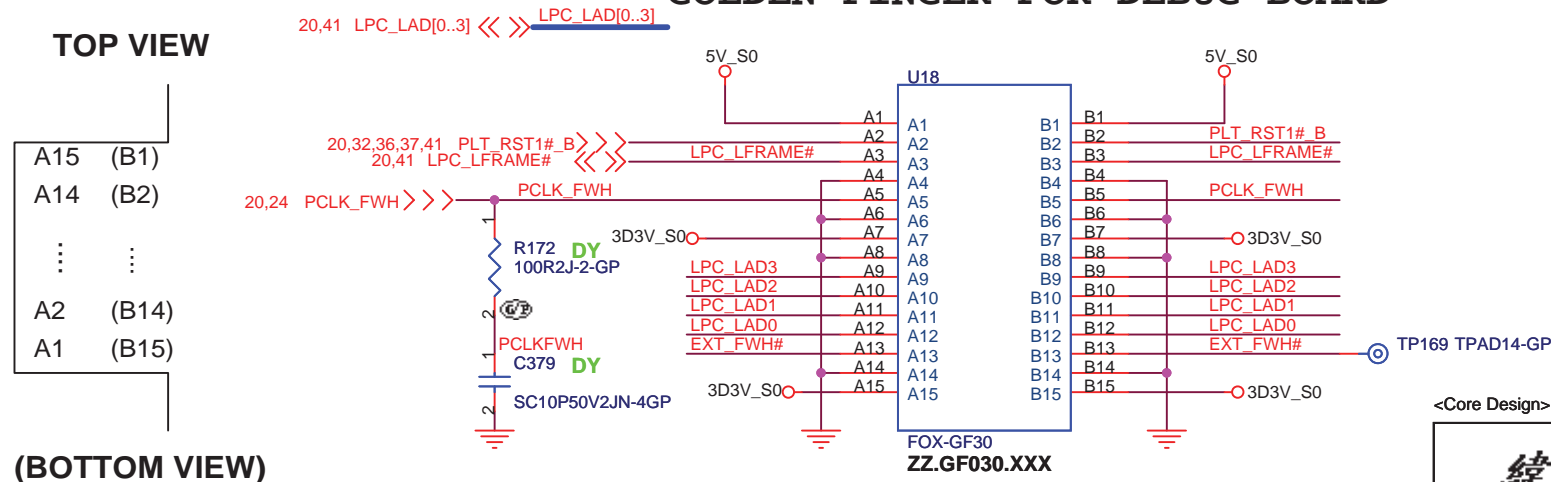
BIOS



CIR Module



GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

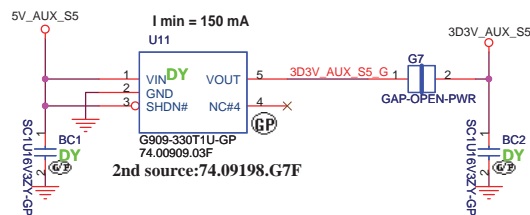
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title **BIOS & CIR**

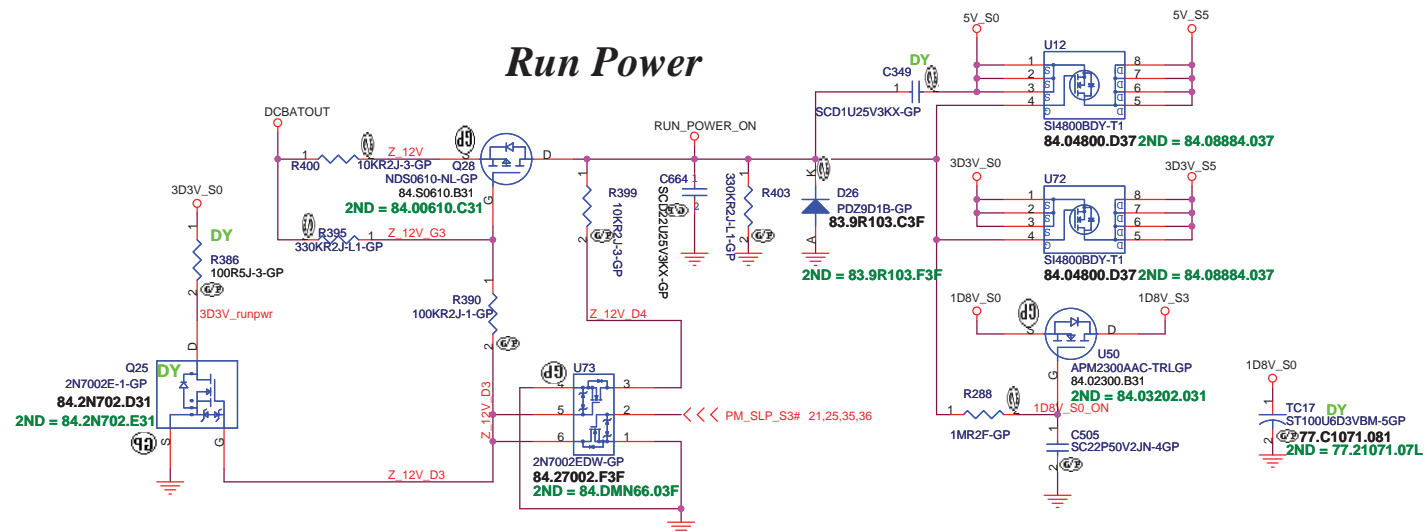
Size A4 Document Number **Big Bear 2A** Rev SB

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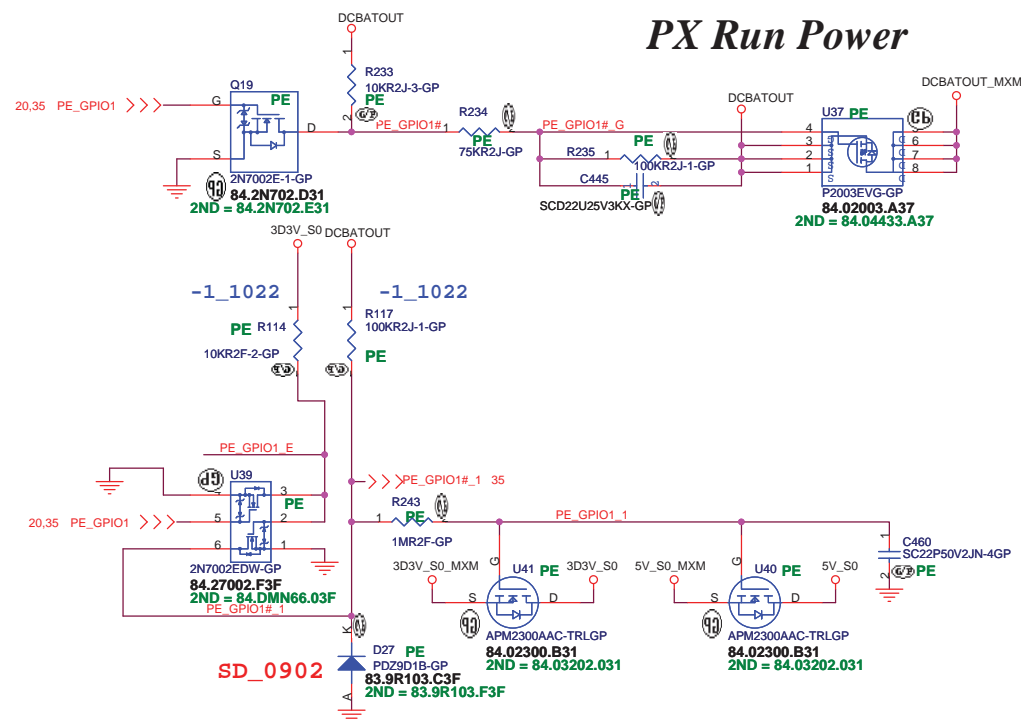
Aux Power 3D3V_AUX_S5



Run Power

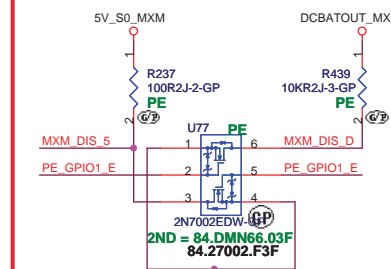


PX Run Power



SD_0902

PX Run Power Discharge circuit



<Core Design>

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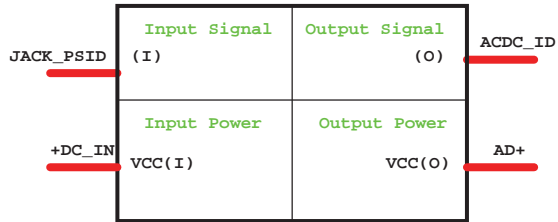
Title	<i>RUN POWER and 3D3V AUX S5</i>
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Size	Document Number	Rev
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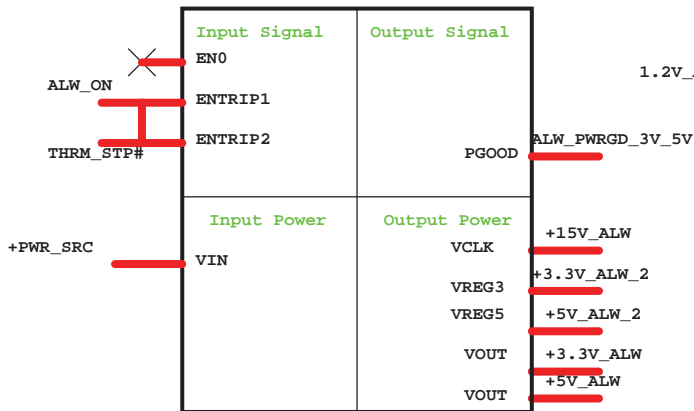
A3 **Big Bear 2A** SD
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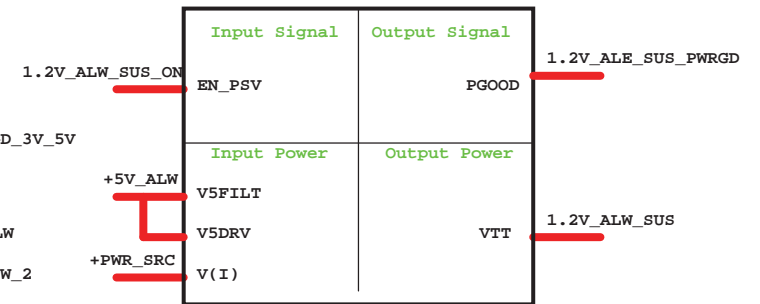
Adapter



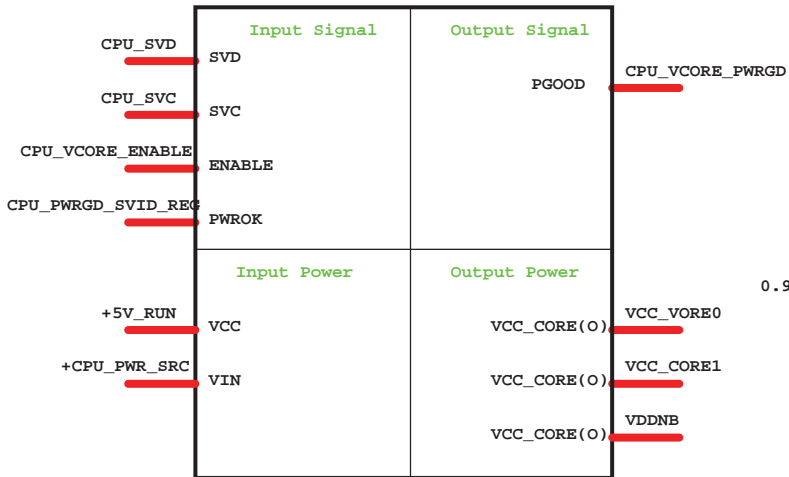
SN0608098



DCDC 1D2V(TPS5117)

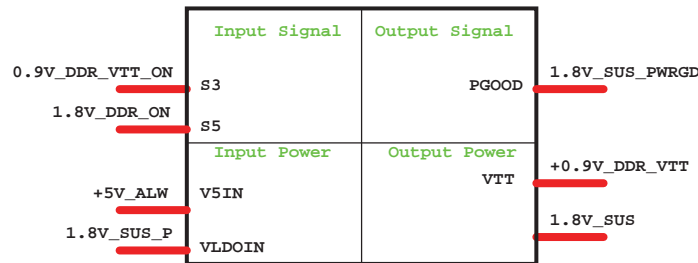


CPU_CORE ISL6265HRTZ

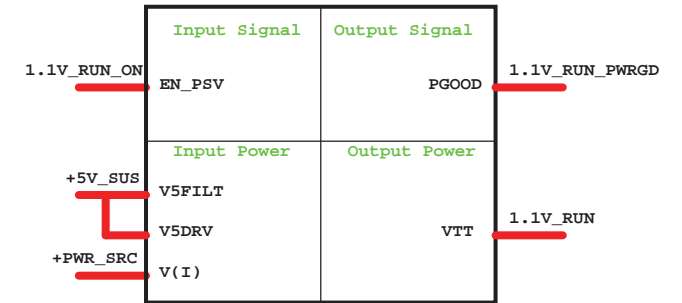


	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	1	1	1
S4	0	0	0	0	0

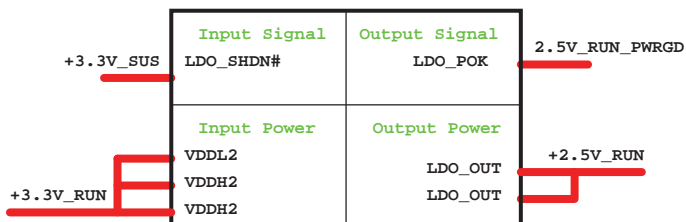
1D8V/0D9V(TPS5116)



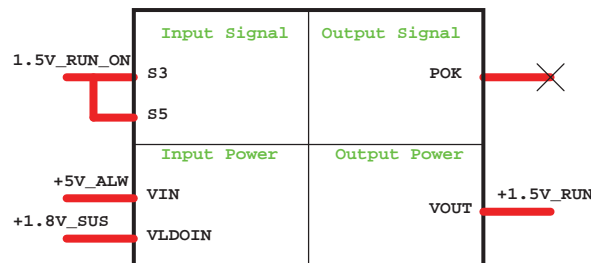
1D1V(TPS5117)



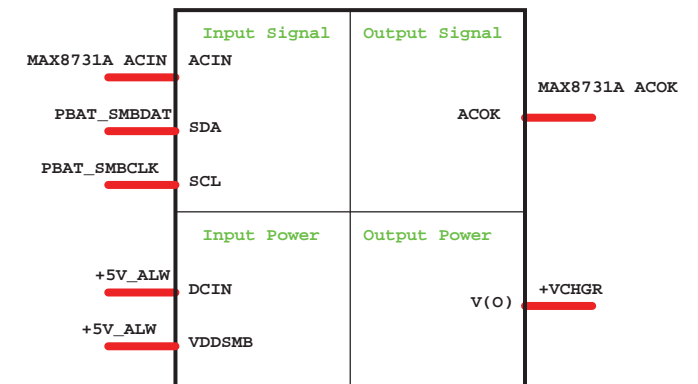
2.5V LDO EMC4002



1.5V_LDO



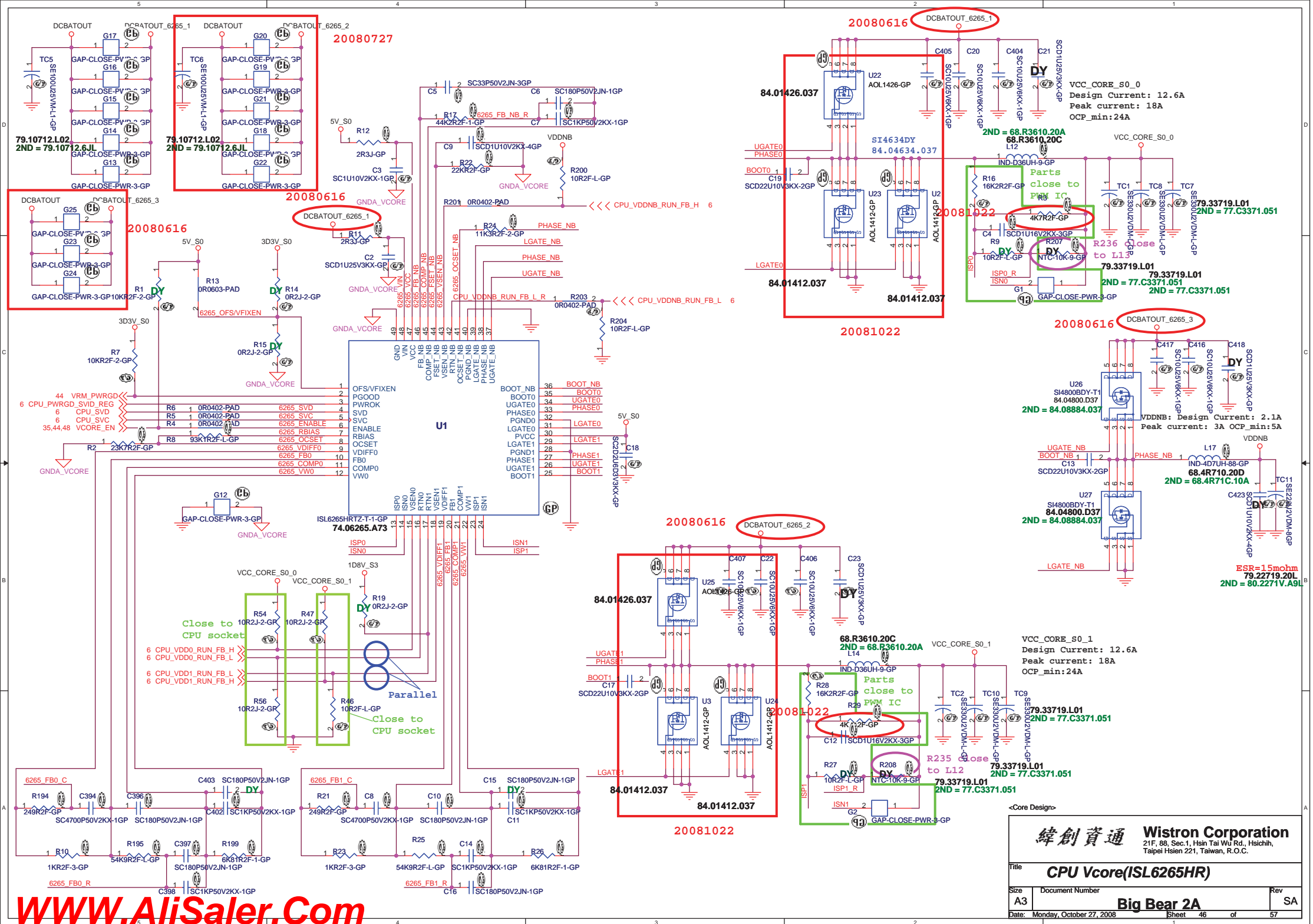
CHARGER BQ24745



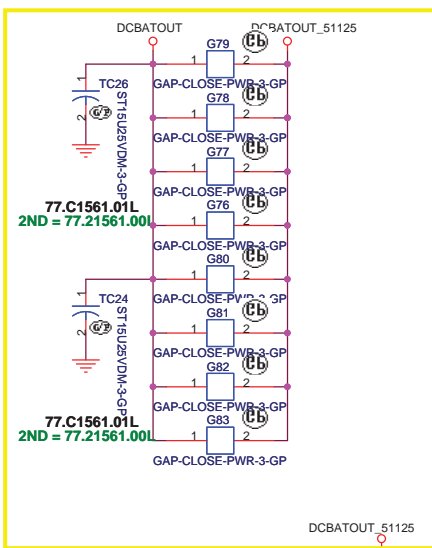
<Core Design>

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Title Power Block Diagram		
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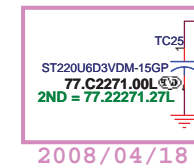
2008/04/15



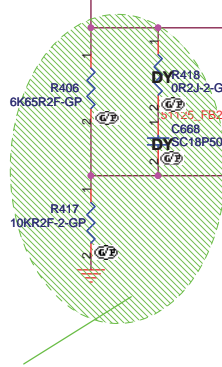
Design Current = 6A
Max Current = 7A
OCP min = 10A

Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A

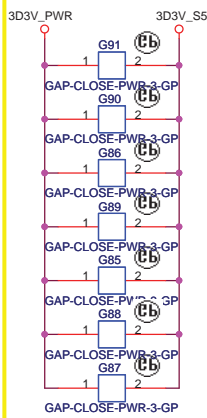
DCBATOUT_51125



2008/04/18



Close to VFB Pin (pin5)



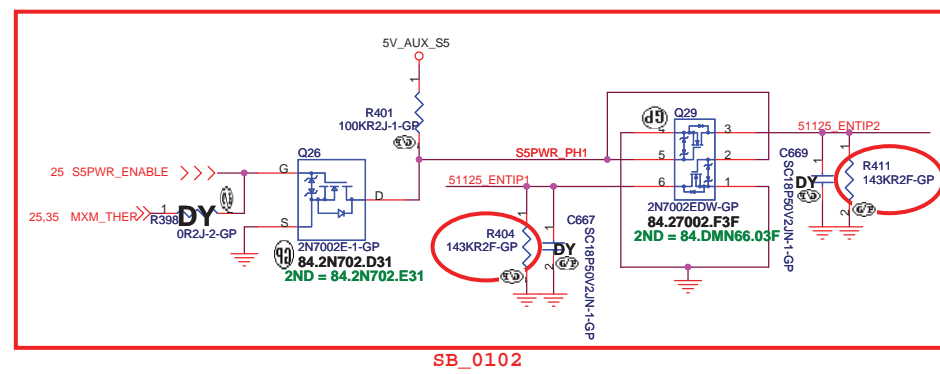
ACOUSTIC NIOSE

Id=7A
Qg=8.7~13nC
84.04800.D37 Rdson=23~30mohm
2ND = 84.08884.037

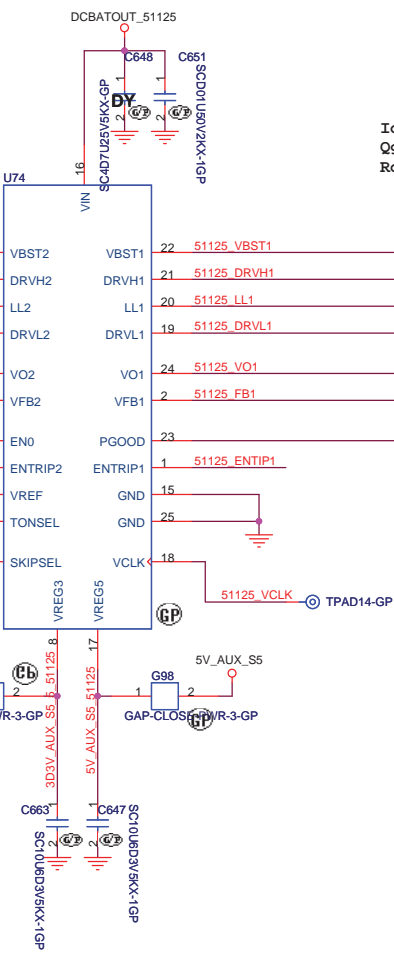
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm

51125_VREF
3D3V_AUX_S5
51125_VREF

3D3V_AUX_S5
-1_1014



SB_0102



Id=7A
Qg=8.7~13nC
Rdson=23~30mohm

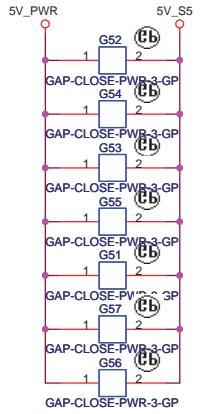
84.04800.D37
2ND = 84.08884.037

Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm

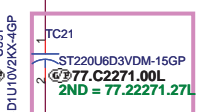
84.04812.A37
2ND = 84.08878.037

51125_VREF
3D3V_AUX_S5
51125_VREF

3D3V_AUX_S5
-1_1014



Design Current = 6A
Max Current = 7A
OCP min = 10A

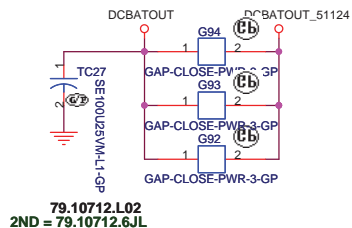


2008/04/18

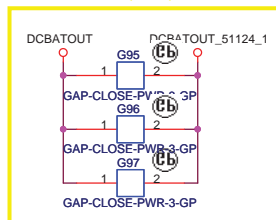
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Title	DCDC 5V/3D3V (TPS51125)		
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A3			
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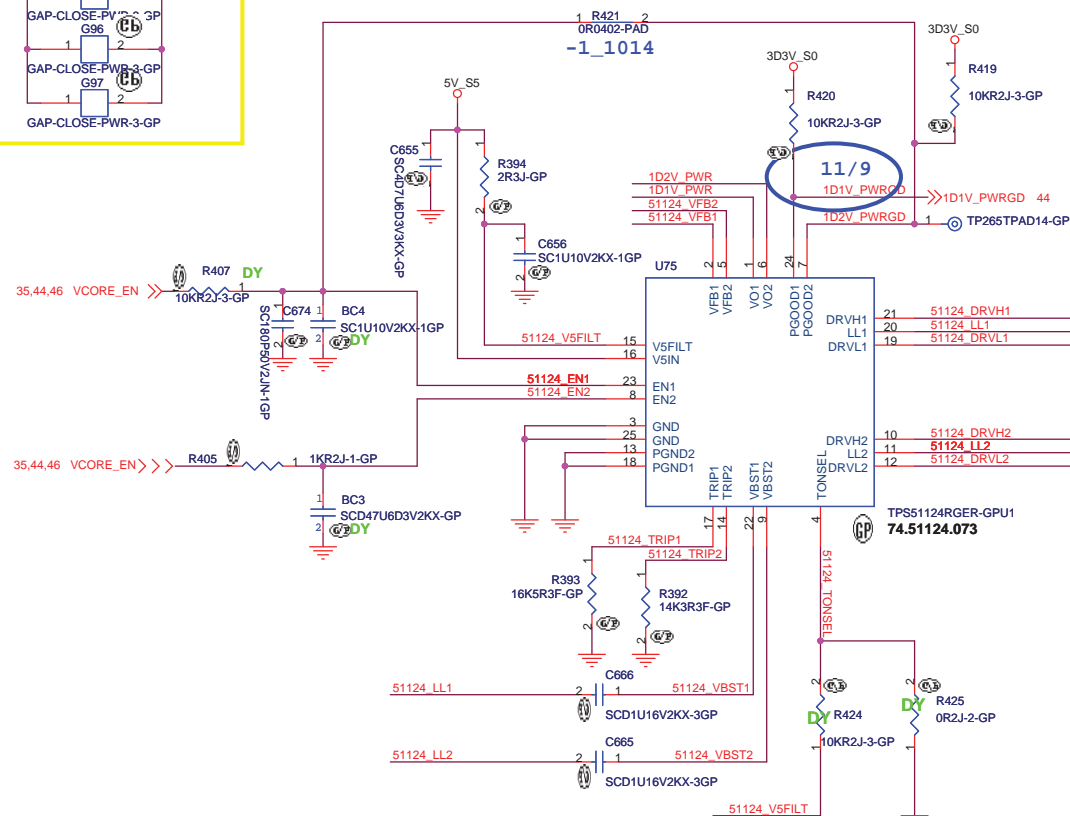


2008/04/17



$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in}))$$

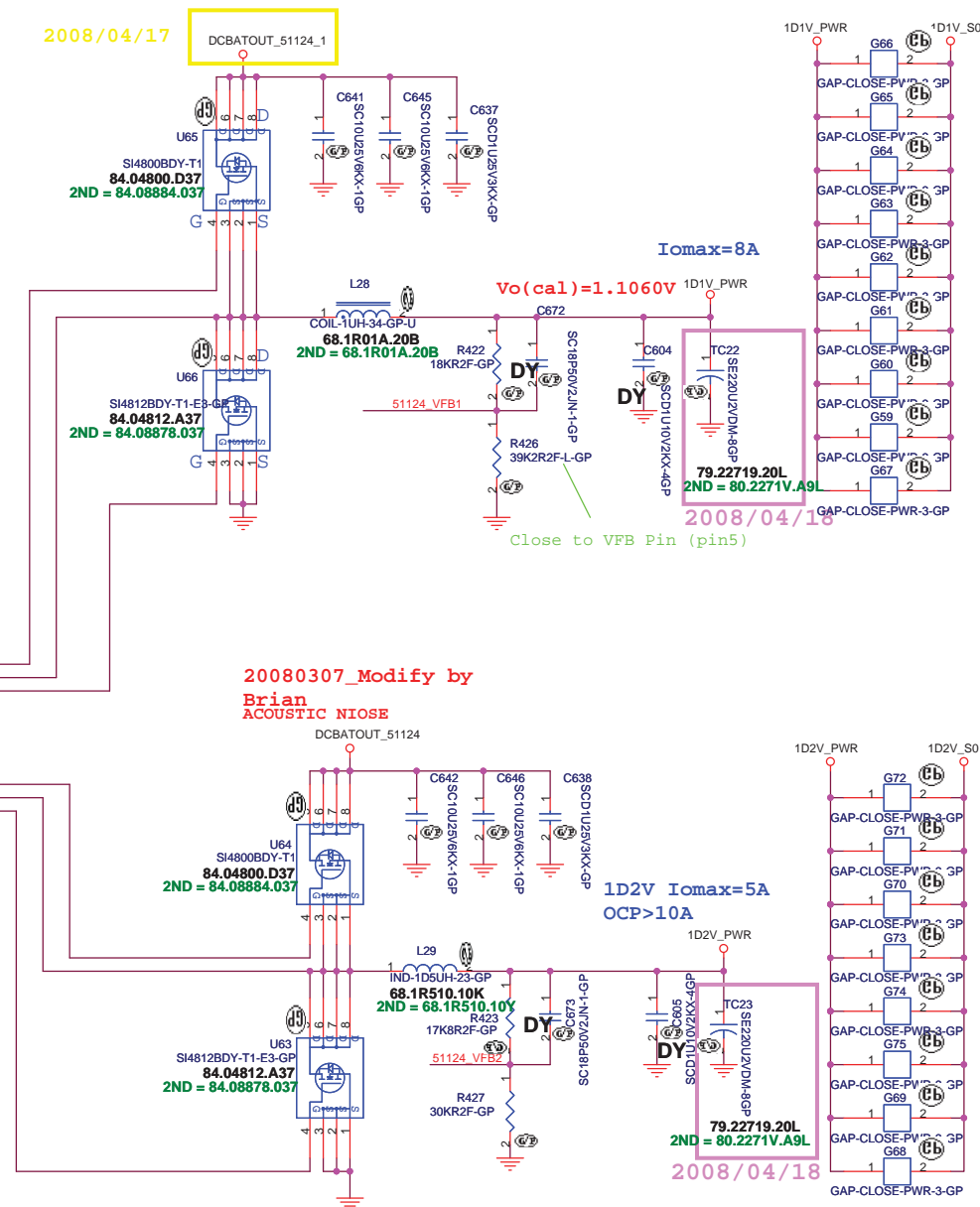


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1+R2)/R2$ --> PWM mode

$V_{out} = 0.764V * (R1+R2)/R2$ --> Skip Mode

2008/04/17



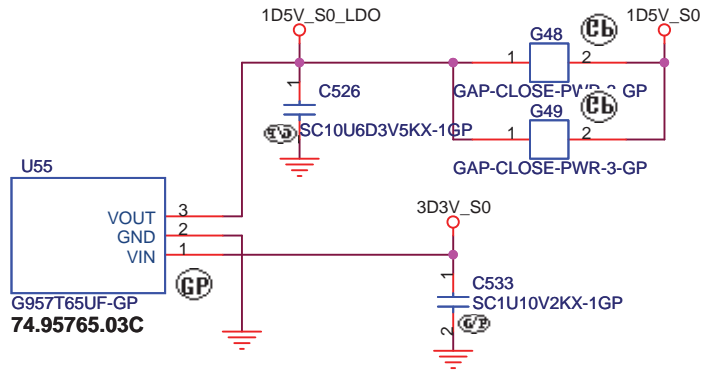
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Taipei Hsien 221, Taiwan, R.O.C.

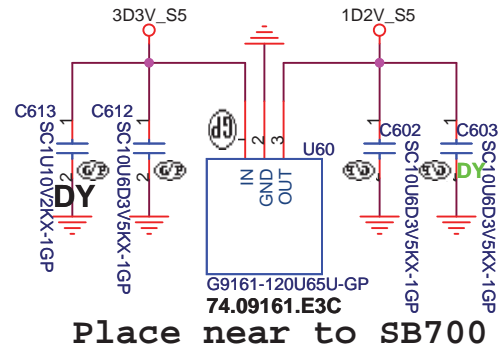
Title			
TPS51124 1D1V 1D2V			
Size	Document Number	Rev	
A3		Big Bear 2A	SA
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G957

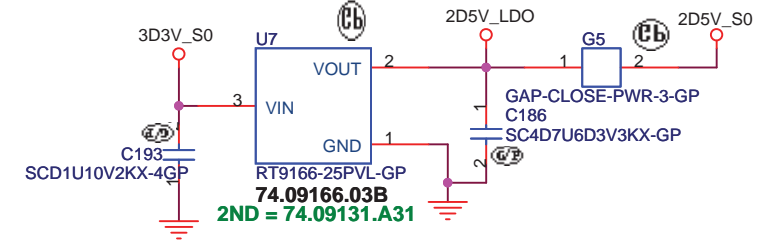
1D5V_S0
I_{omax}=1A



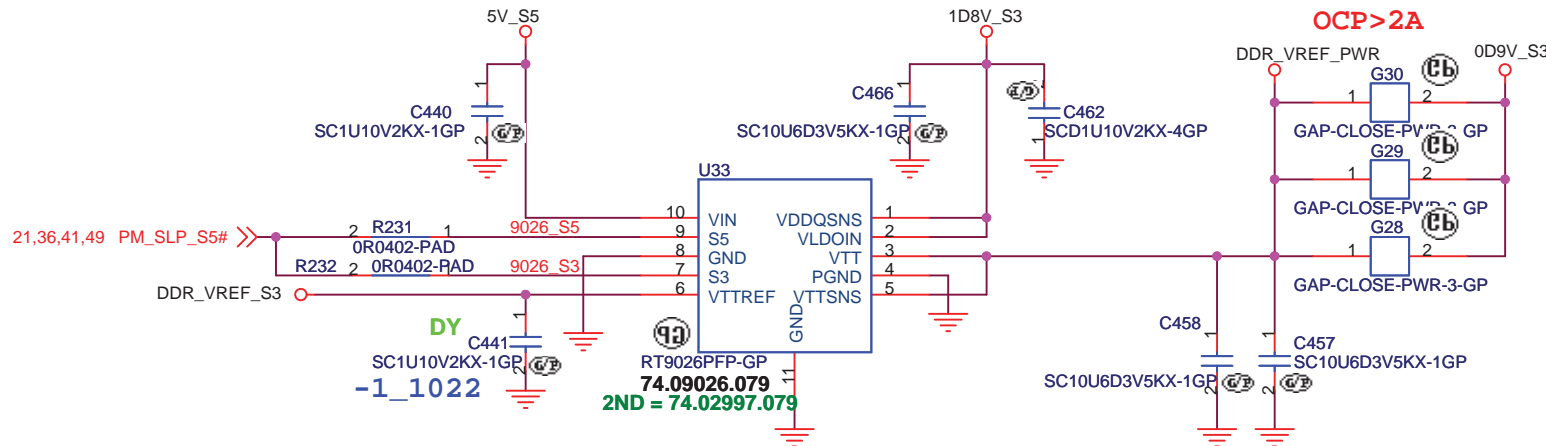
1D2V_S5
I_{omax}=400mA



2D5V_S0
I_{omax}=0.3A 2D5V/300mA



I_{omax}=1A
OCP>2A



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

0D9V&2D5V&1D25V&1D5V

Size

Document Number

A4

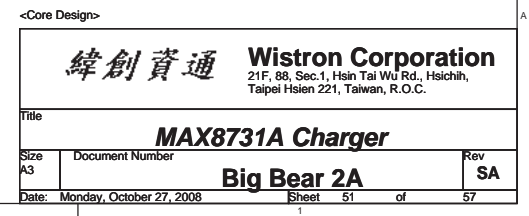
Big Bear 2A

Rev

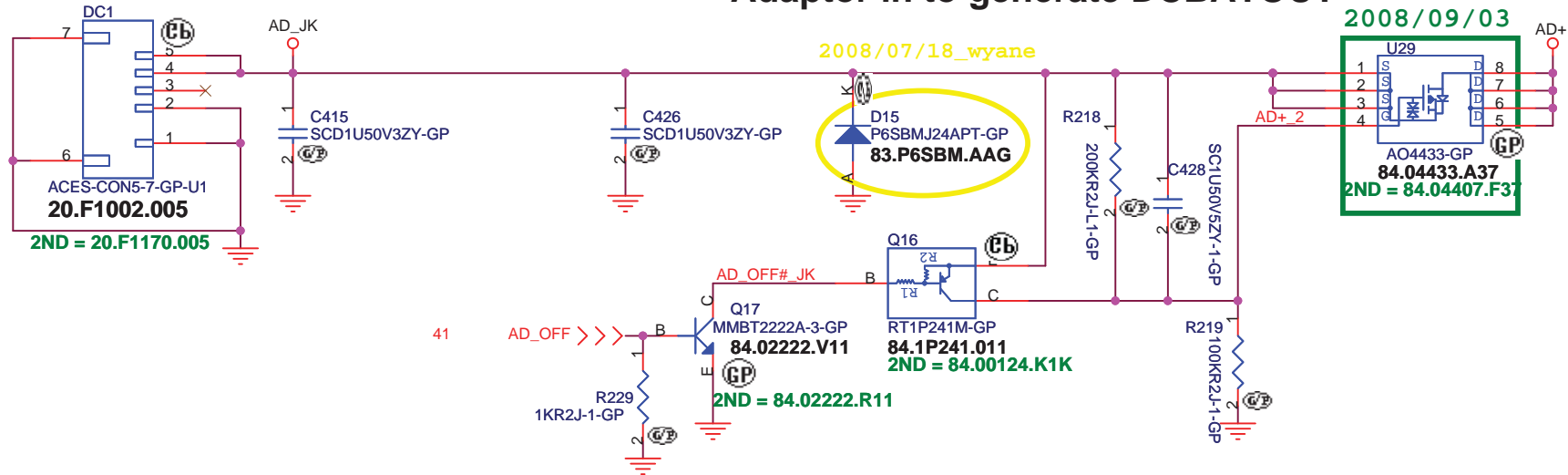
SB

Date: Monday, October 27, 2008

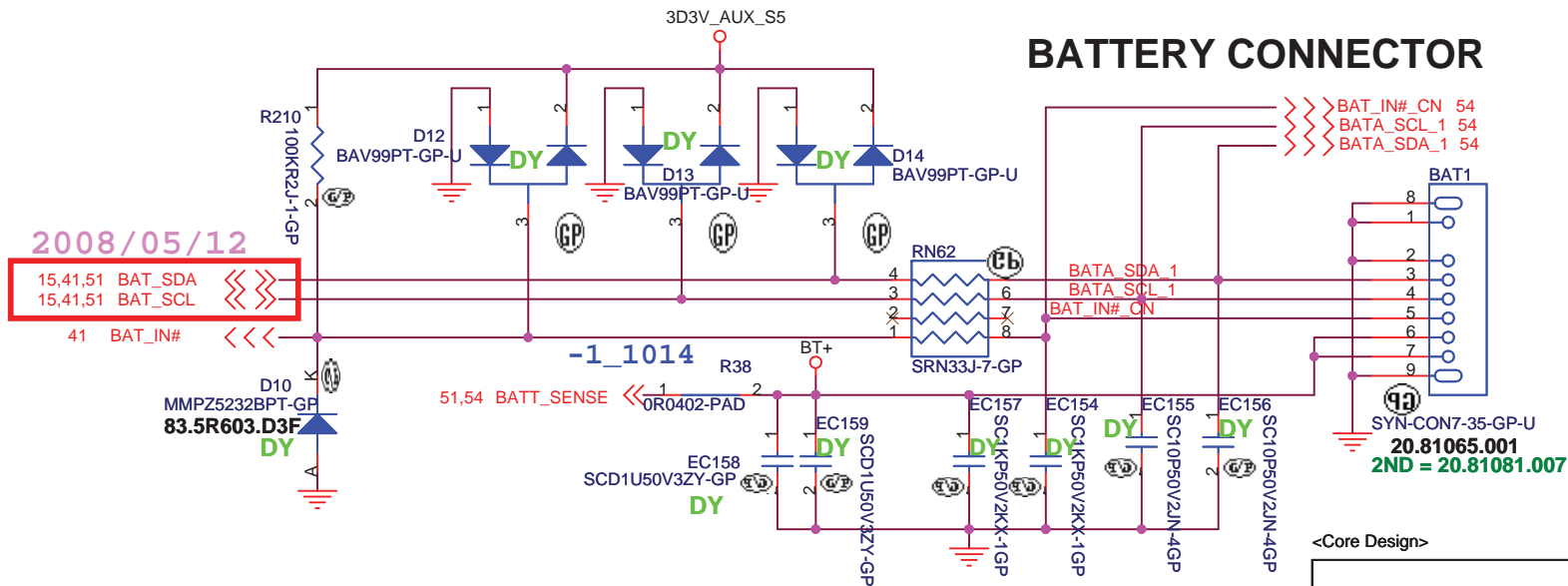
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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

緯創資通

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Title

AD/BATT CONN

Size
A4

Document Number

Big Bear 2A

SA

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